

The Future of Microelectronics Technology

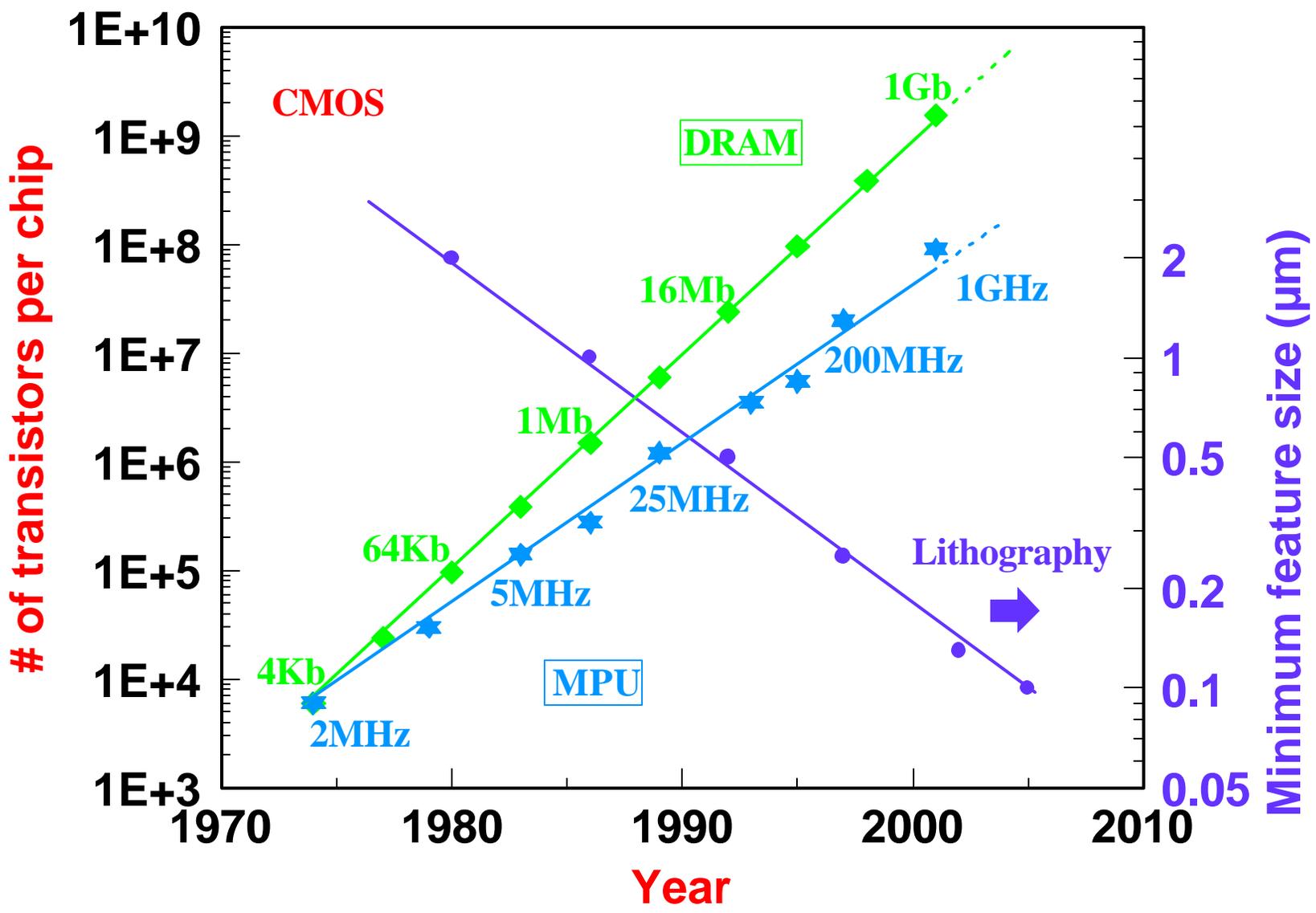
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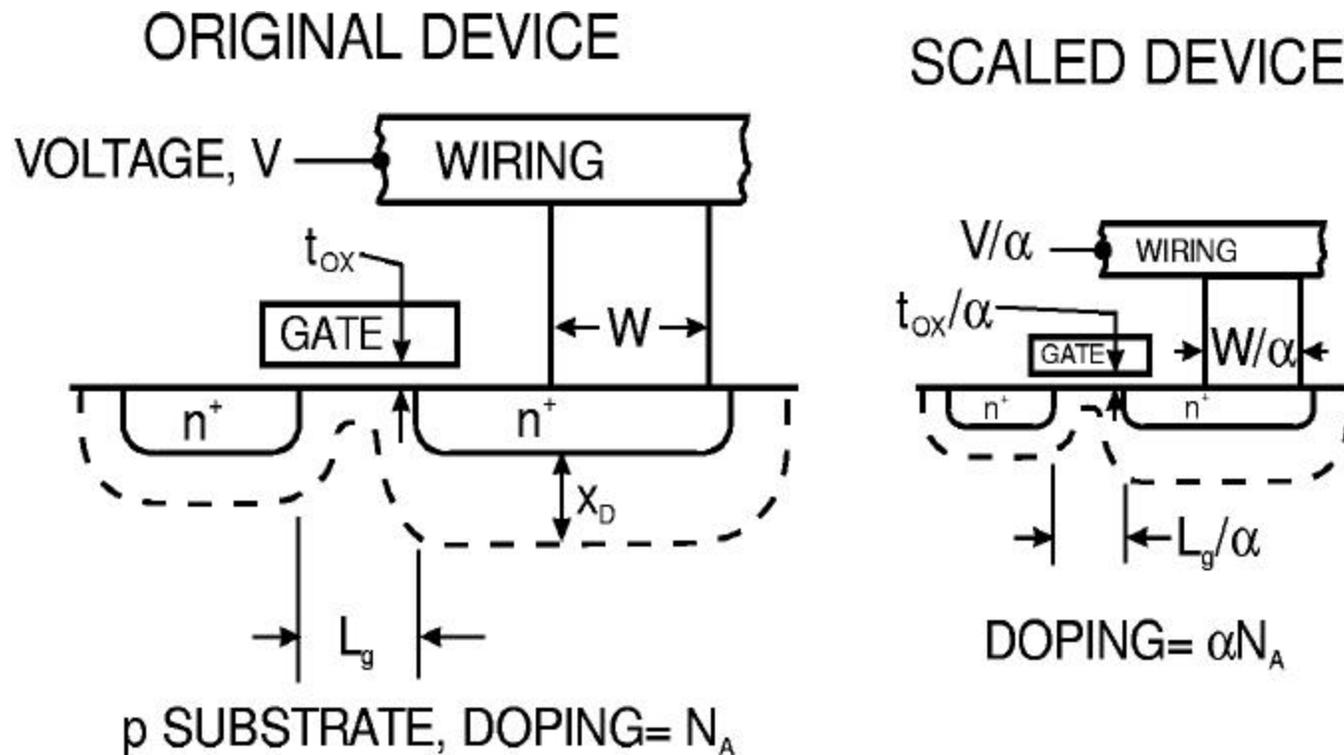
OUTLINE

- **A Brief History of CMOS VLSI**
- **Impending Issues on Further Scaling**
 - ▶ **Lithography**
 - ▶ **Voltage Limits**
 - ▶ **Oxide Tunneling**
- **Alternative Materials and Device Structures**
 - ▶ **High-k Gate Dielectric**
 - ▶ **SOI**
 - ▶ **Double-Gate MOSFET**
- **Emerging System Applications**
 - ▶ **Low Power**
 - ▶ **RF System on a Chip**
 - ▶ **Photo Detector Arrays**

VLSI Density and Feature Size vs. Time

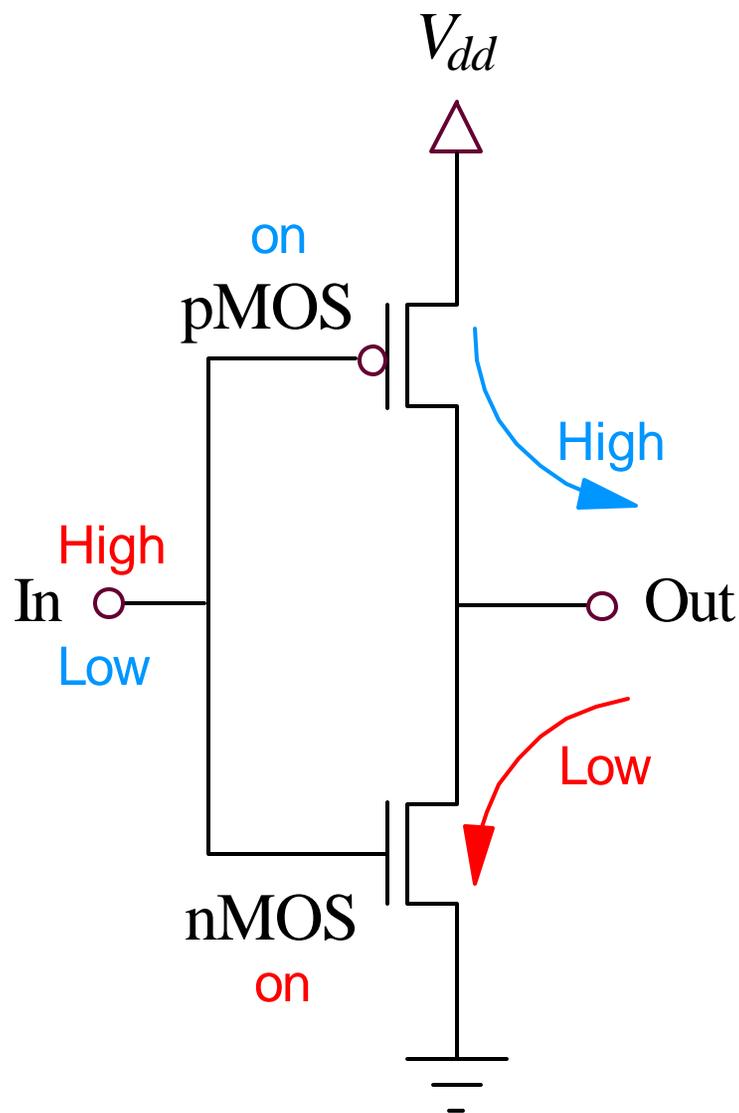


MOSFET Scaling



- Currents scale as $1/k$; Capacitances scale as $1/k$.
- Gate delay scales as $1/k$.
- Power per circuit scales as $1/k$.²

The Magic of CMOS Circuit



- Negligible standby power dissipation.
- Focus all power budget to switching events.
- Key to VLSI integration with low activity factors.
- The only known circuit with such properties.

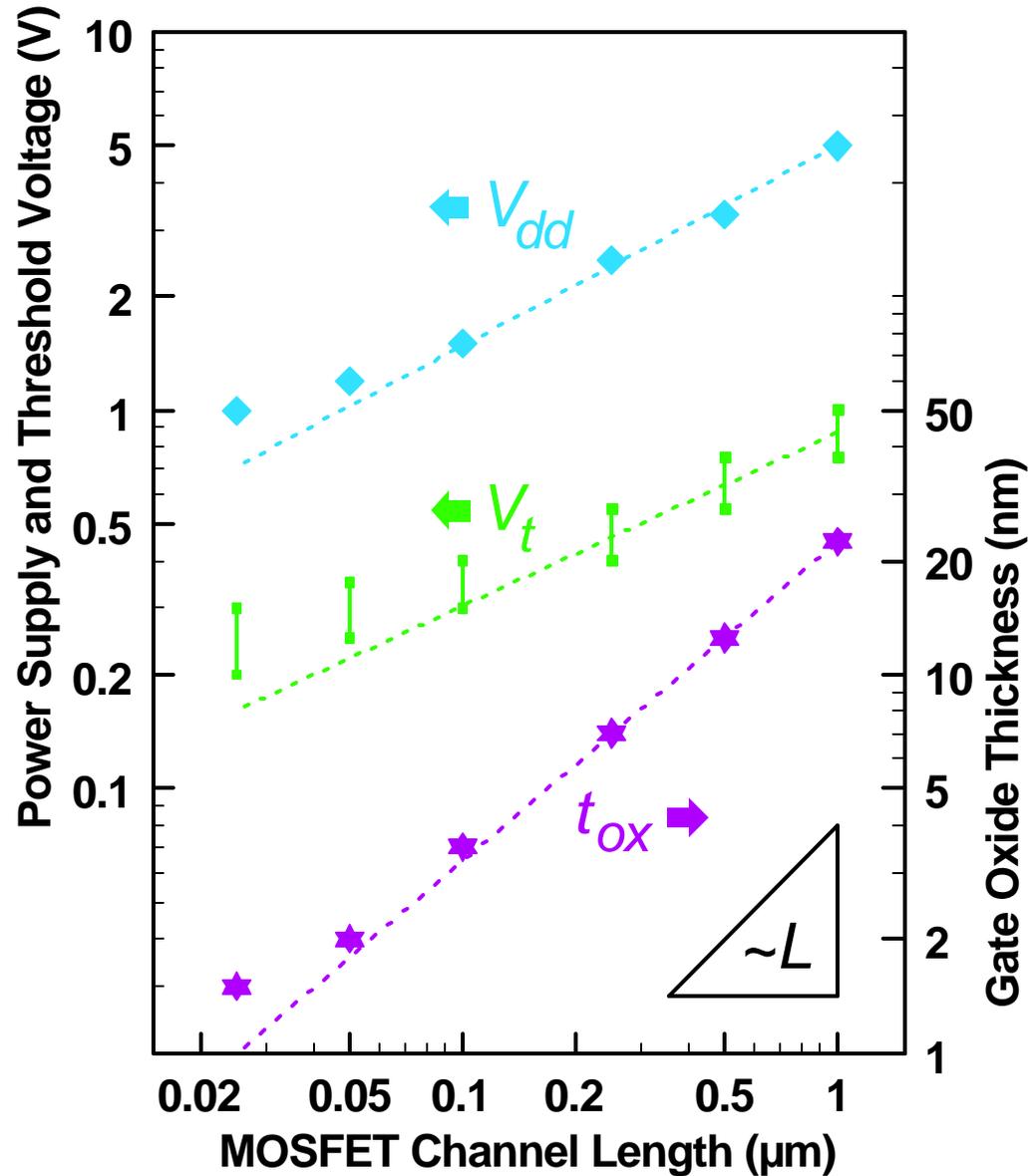
Impending Issues on Further Scaling

- **Lithography**
- **Voltage Limits**
- **Oxide Tunneling**
- **Dopant Number Fluctuations**

Enabling Technologies for VLSI

- **Lithography**
- **Ion Implantation**
- **Reactive Ion Etching**
- **Rapid Thermal Annealing**
- **Chemical Vapor Deposition**
- **Chemical-Mechanical Polishing**

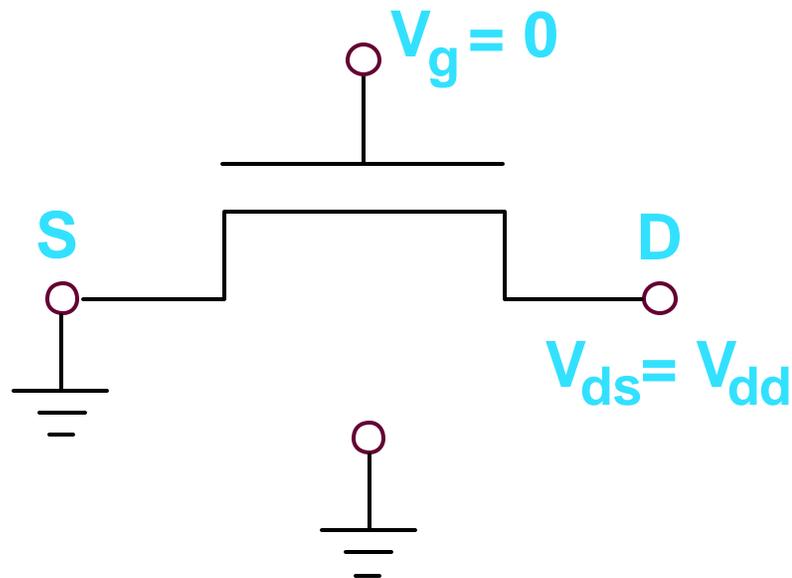
CMOS Scaling Trends



- We are already at 50 nm today.
- Likely to extend to 20-25 nm.
- $L = 10$ nm unattainable?

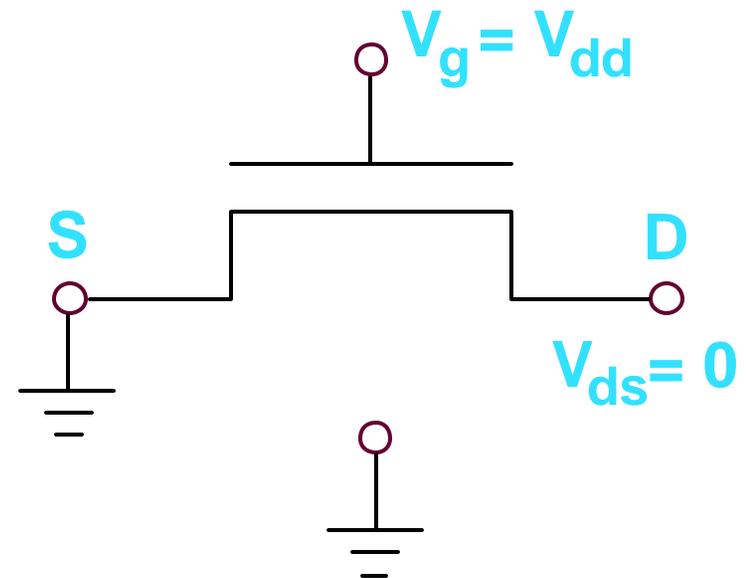
Limits to MOSFET Scaling

Standby: OFF



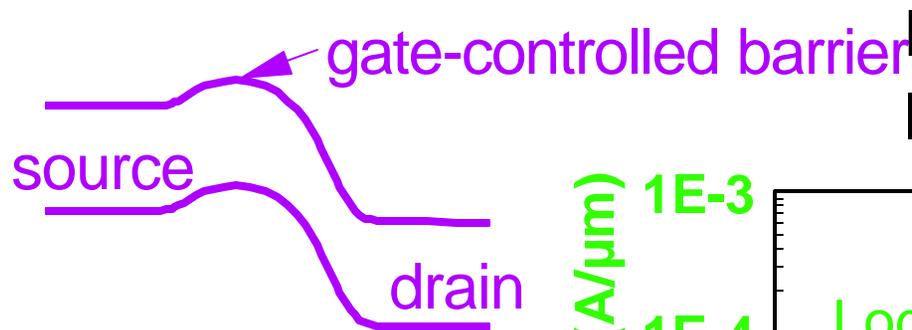
- Thermal injection over source-to-drain barrier.
- Band-to-band tunneling from drain to body.
- Tunneling through source-to-drain barrier.

Standby: ON

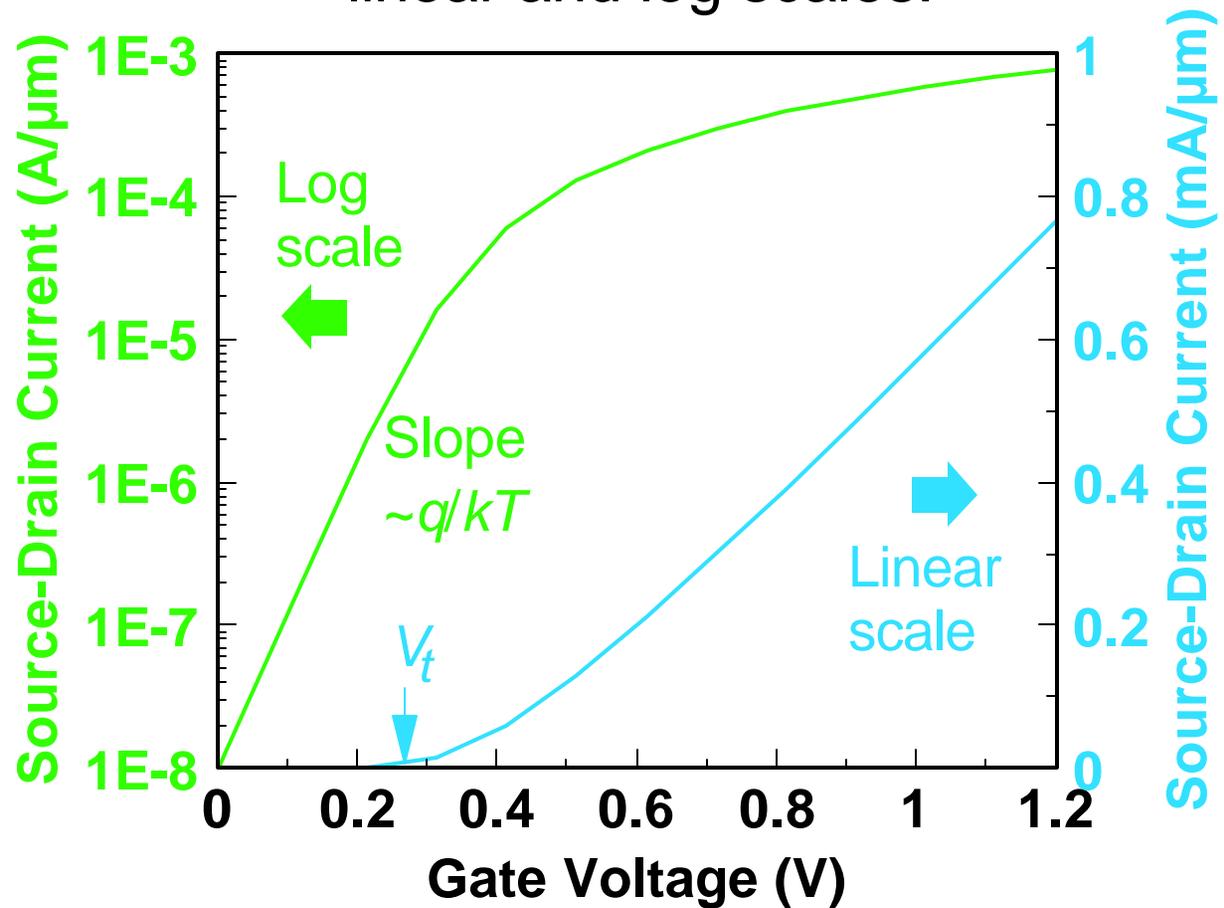


- Tunneling through gate oxide.

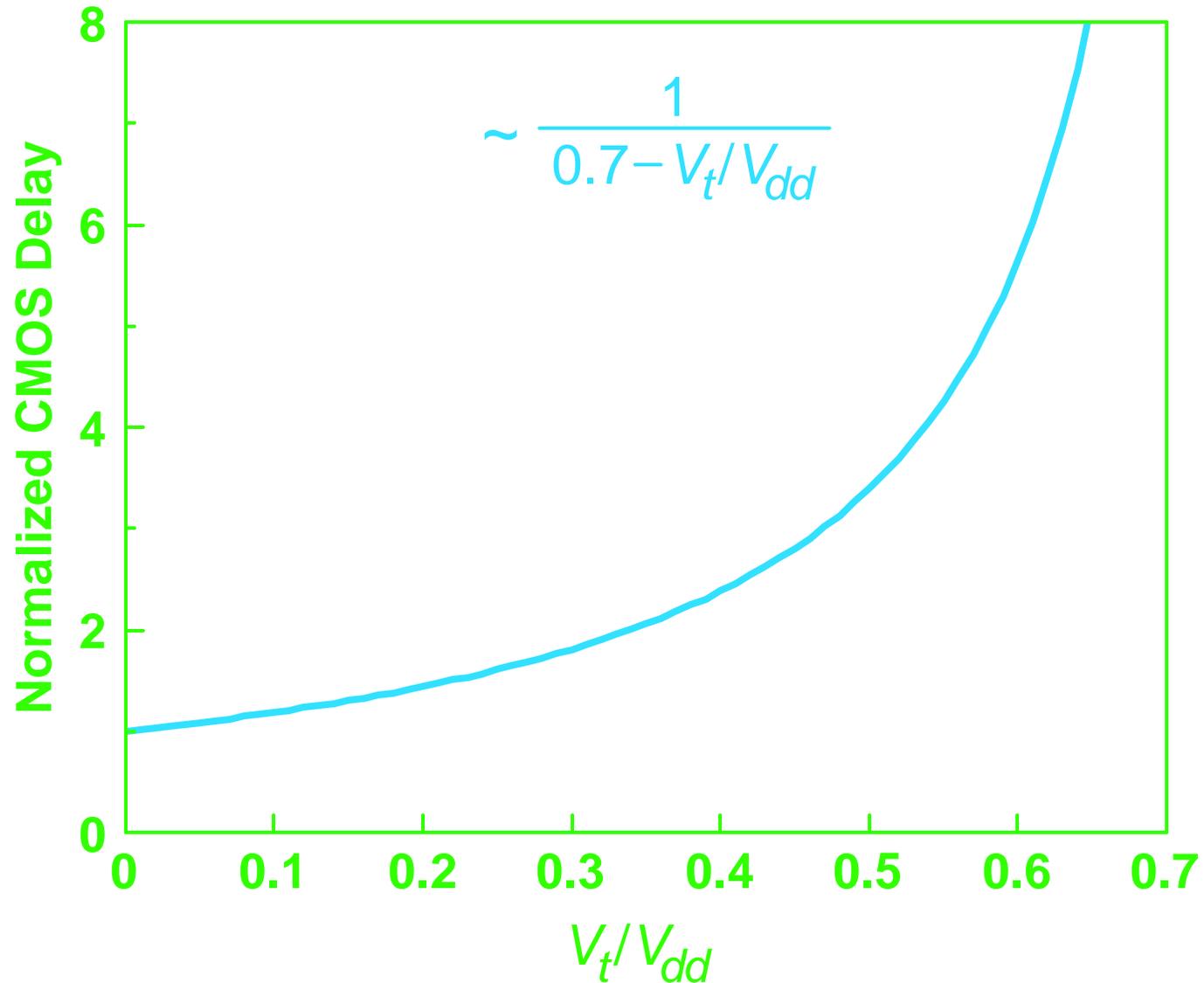
Subthreshold Non-Scaling



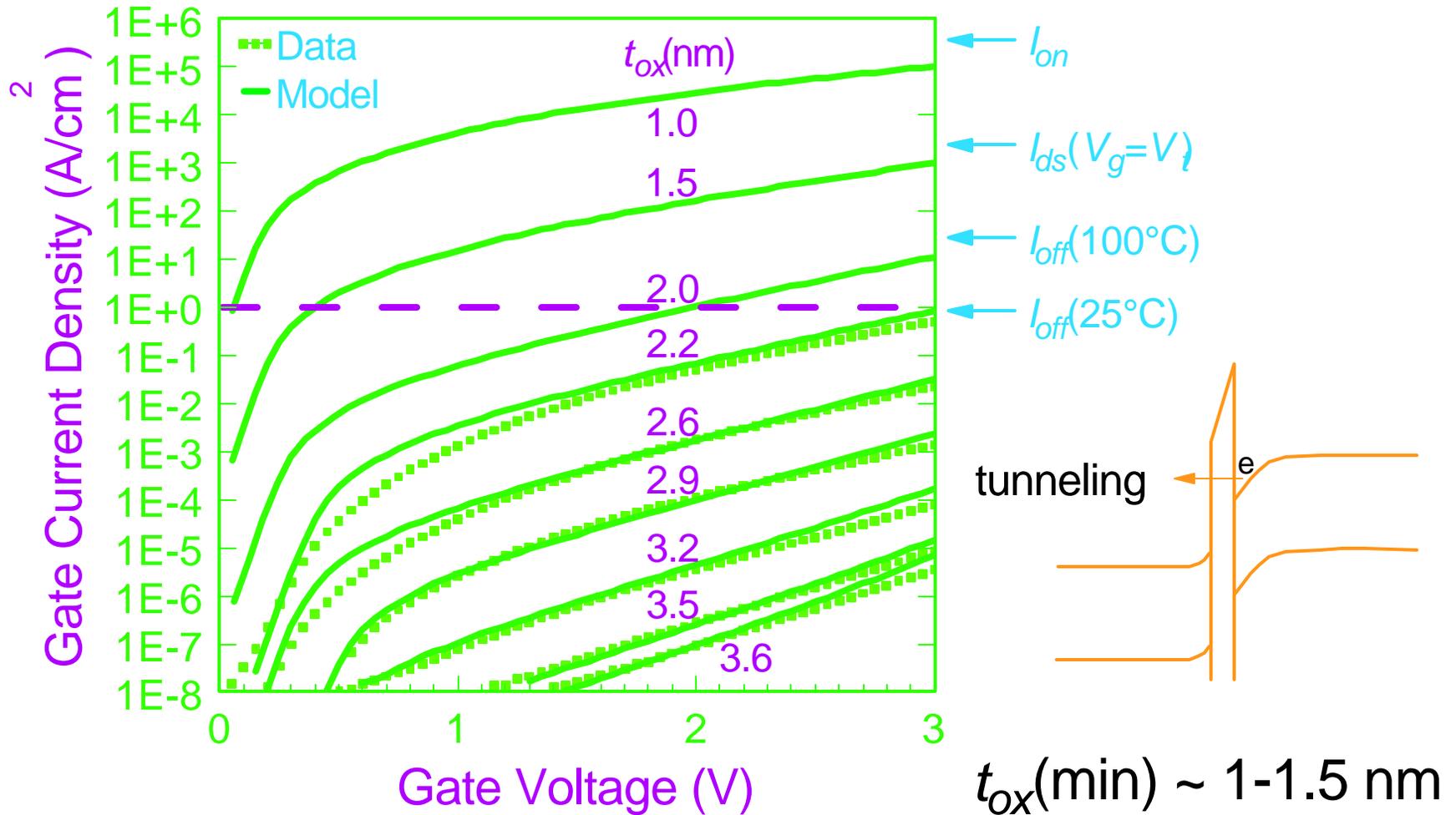
MOSFET current in linear and log scales:



CMOS Delay as a Function of V_t/V_{dd}



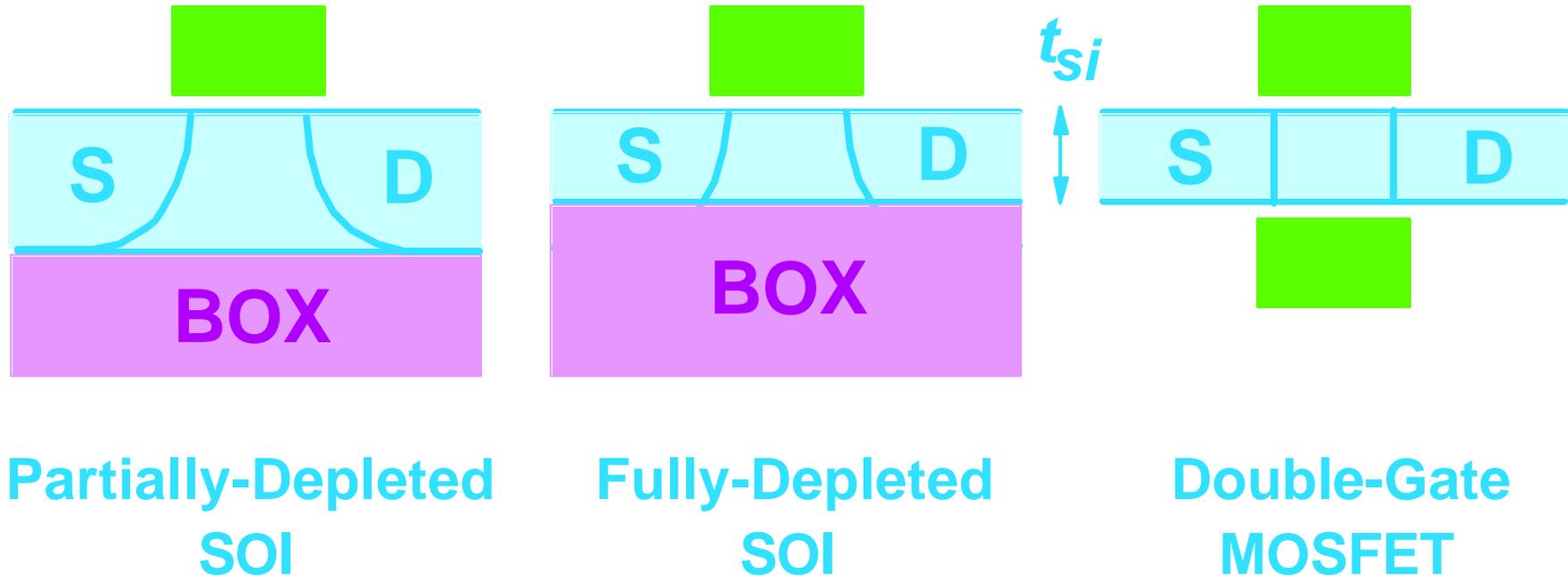
Gate Oxide Tunneling



Alternative Materials and Device Structures

- **High-k Gate Dielectric**
- **Strained Si/SiGe**
- **SOI**
- **Double Gate MOSFET**

Other MOSFET Device Structures

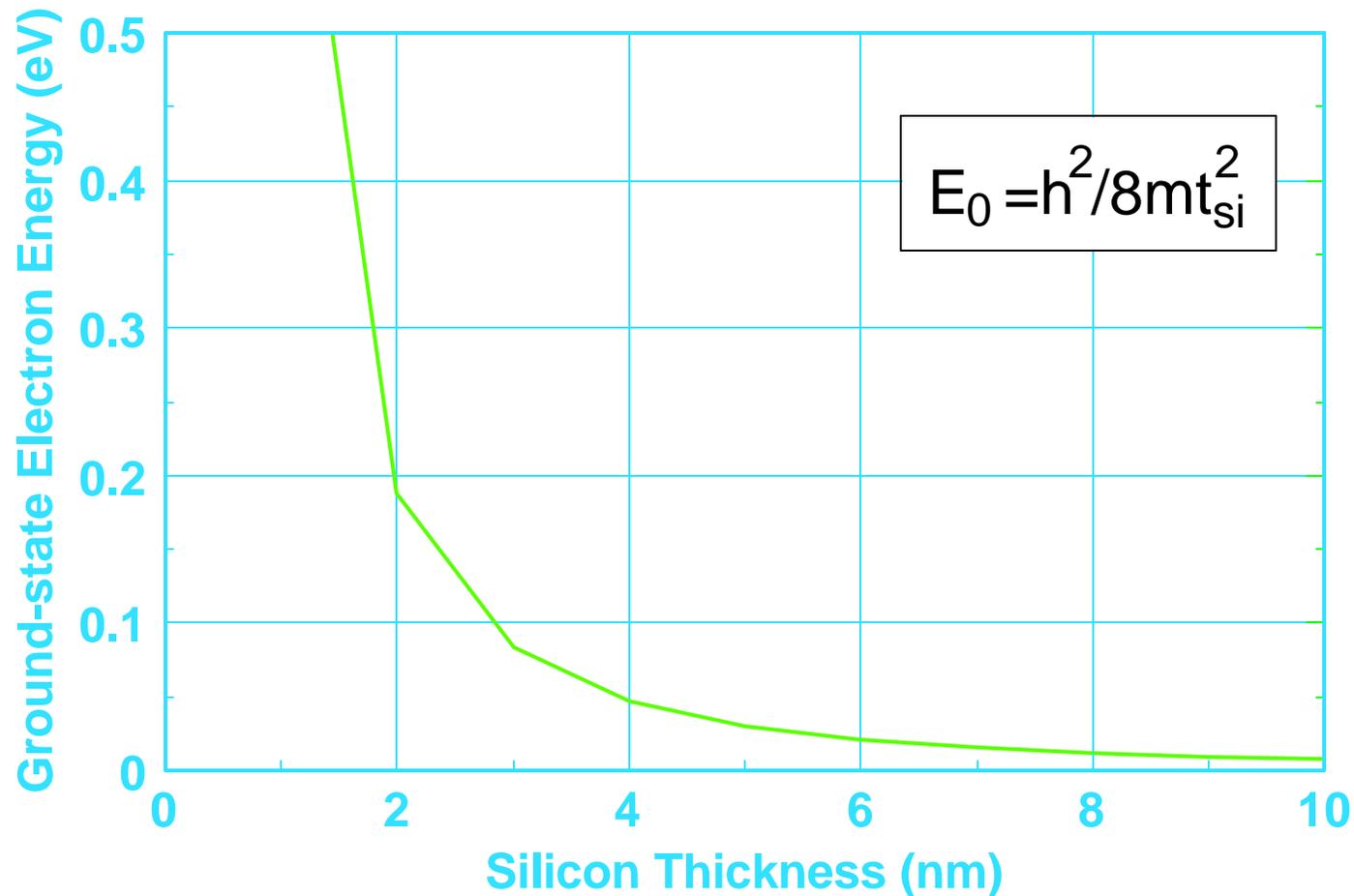


- Partially depleted SOI has the same scaling limits as bulk CMOS.
- Scaling of fully-depleted SOI and double-gate MOSFET depends on the thickness of the silicon film.

Fabrication Challenges of Double-Gate MOSFET

- Both the front gate and the back gate must be self-aligned to the source-drain and to each other.
- Silicon film thickness must be less than $\sim L_{gate} / 3$ (< 10 nm) with tight control (< 1 nm).
- Need source-drain fan-out (self-aligned to the gates) to reduce series resistance as well as thermal resistance.
- Threshold voltages dictated by gate work functions, difficult to make multiple threshold voltages on a chip.

How Thin Can the Silicon Film Be?



- V_t shifts to higher values due to quantum confinement.
- Difficult to use silicon films thinner than 3-4 nm.

Emerging System Applications

- **Merged Logic and DRAM**
- **Low Power**
- **RF System on a Chip**
- **Detector Arrays**

Low Power Electronics

- Applications/System Needs
 - Palm PDA's, Smart phones, etc.
 - Speech recognition
 - DSP, video encoding
 - Integrate SDRAM, analog, processor
- Low Power Features
 - 100 MHz, < 1 V logic ckts.
 - Multiple V_t , V_{dd}
 - Active triple well, dynamic V_t
 - Header/Footer for disabling macros
 - Optimum device width vs. C_{wire}

CONCLUSION

- **Lithography will be scaled to 100 nm linewidth in about 2005, but uncertain after that.**
- **Due to oxide and voltage (power) limits, CMOS devices will reach a limit at 10-20 nm channel length.**
- **No alternate devices on the horizon can replace CMOS in the VLSI market.**
- **The future of microelectronics lies more in the system application areas, e.g., Low power electronics, RF CMOS, Optoelectronics, etc.**