

**MICROELECTRONICS :
NEW TECHNOLOGY
for NEW PHYSICS**

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MICROELECTRONICS SCHOOL

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**COMPONENTS IN
EXPERIMENT**

TRACKING

GASEOUS DRIFT / WIRE CHAMBERS
SEGMENTED SILICON ARRAYS
SCINTILLATING FIBERS

MUON DETECTION

GASEOUS WIRECHAMBERS

**MAGNETIC FIELD
DEFLECTION**

CALORIMETRY

IONIZATION (LIQ A)
HEAVY CRYSTALS
SCINTILLATION --> HYBRID

IDENTIFICATION METHODS

IONIZATION DENSITY
CERENKOV EFFECT --> RICH

DATA ANALYSIS

ON - LINE and OFF - LINE



CONTENTS

**MICROELECTRONICS
ENABLING TECHNOLOGY**

SIGNAL PROCESSING

10^8 s^{-1}

GRANULARITY

$1 \text{ cm}^{-2} \rightarrow 10^4 \text{ cm}^{-2}$

SYSTEM HOUSEKEEPING

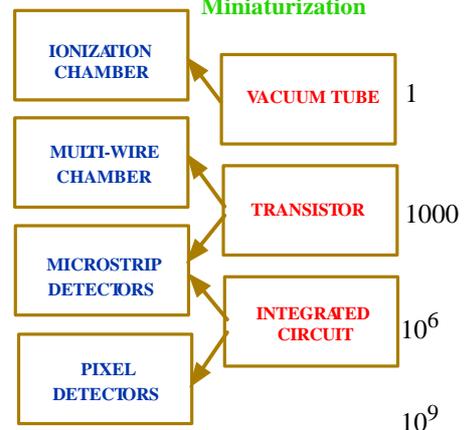
PACKAGING and 3-D



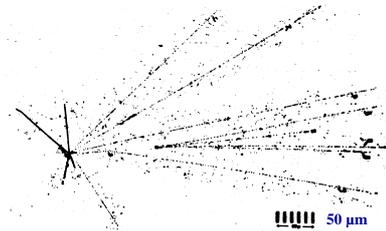
**DETECTOR SEGMENTATION
and ELECTRONICS READOUT**

Segmentation

**ELECTRONICS
Miniaturization**



EVENT RECONSTRUCTION



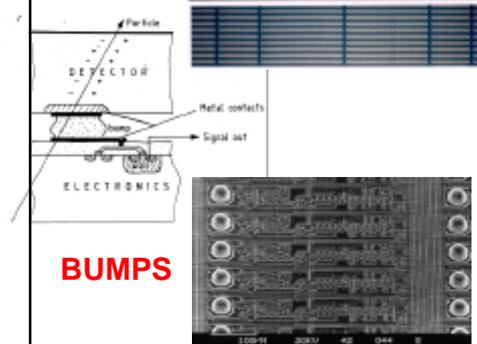
Emulsion Event WA59 ~ 1985

TIMING of EVENTS
POSITIONS --> TRACKS
TRACK LENGTH --> LIFETIME
MOMENTUM / ENERGY
PARTICLE IDENTIFICATION
STATISTICS / SELECTIVITY

PIXELS in PARTICLE PHYSICS HYBRID Si SENSOR

SENSOR MATRIX

Si

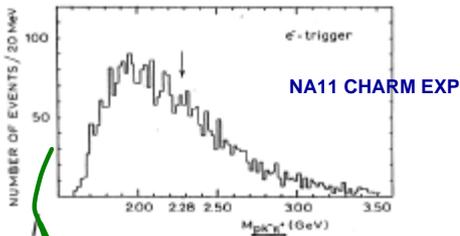


BUMPS

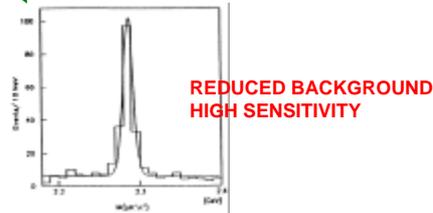
READOUT ELECTRONICS

PARTICLE RECOGNITION

INVARIANT MASS DISTRIBUTION
LARGE STATISTICS / 'NO' SELECTIVITY

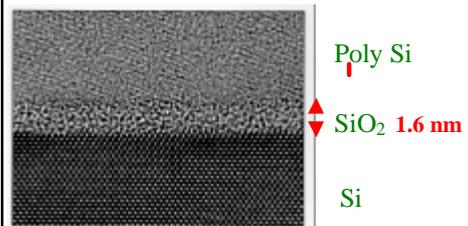


NEW TECHNOLOGY :
 Si MICROSTRIP DETECTORS



Impact Deep-submicron CMOS for ADVANCED detector readout

MOS Gate TEM Bell Labs April 2000

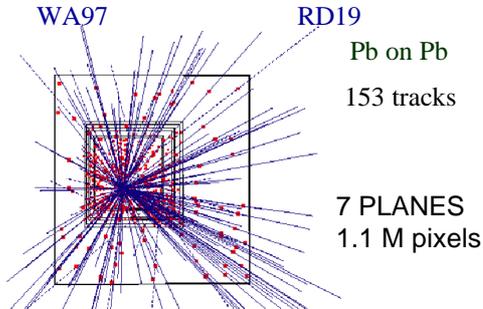


Reliable oxides can be made already with only ~ 6 atoms in SiO₂ layer

SiO₂ CMOS technology used for 0.08 μm --> 0.02 μm? transistors
 --> "Noon Lecture" by TAUR

Thin gate oxide (< 8 nm) also is unaffected by radiation (test > 30 Mrad)

TRACKING with PIXELS at CERN

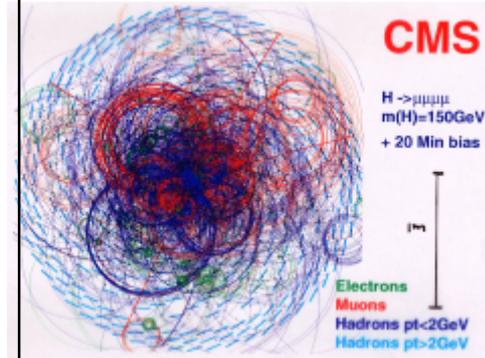


PIXEL DETECTORS FOR TRACKING :

DAMERELL : TUESDAY NOON
'SCHOOL' WEDNESDAY

FUTURE EXPERIMENTS

PROTON & HEAVY-ION COLLIDER expts
 HIGH MULTIPLICITY hundreds per event
 HIGH RATE 40 MHz -> 80 MHz



HIGHLY SEGMENTED, FAST,
 RADHARD DETECTORS NEEDED
 CRYOGENIC --> RADHARD

IMPACT of TECHNOLOGY

MICROELECTRONICS

DATA PROCESSING CAPABILITY <----
 SENSOR ARRAY TECHNOLOGIES (CCD, Si, GaAs,)
 READOUT AND SIGNAL PROCESSING
 RF TECHNIQUES
 HOUSEKEEPING OF SYSTEM FUNCTIONS

MORE GRANULARITY

OPTO - ELECTRONICS

OPTICAL FIBERS
 SIGNAL TRANSMISSION ON-CHIP AND OFF-CHIP

'PACKAGING' TECHNIQUES

HYBRIDIZATION
 3 - D SENSORS AND PROCESSORS

MICRO - MECHANICS

Si, Carbon STRUCTURES

IEEE ACTIVE IN THIS AREA

PROCEEDINGS of the IEEE in 2000, 2001
 LOW POWER, LIMITS, INTERCONNECTIONS

FUTURE EXPERIMENTS

ELECTRON or MUON COLLIDER expts
 MODERATE MULTIPLICITY
 < hundred per event
 LOW RATE Hz - kHz

TRACKING NEEDS (Damerell 10 July)

HIGH PRECISION ~1 μm
 --> SMALL SEGMENTS
 THIN DETECTORS
 SIGNAL in 25 μm Si : 2000 e^- ~ 7 keV
 --> LOW NOISE < 60 e^- rms

IN VACUUM

CCD or CMOS IMAGERS may work
 CRYOGENIC OPERATION for low noise

SEGMENTATION

INCREASING GRANULARITY
IMPROVES not only
PHYSICS DATA but
also DETECTOR
CHARACTERISTICS
INTRINSIC RELATIONS between
SPEED, POWER, NOISE,
CAPACITANCE
SIGNALS usually UNCHANGED
LITTLE LATERAL EXTENSION

POSSIBLE by
MINIATURIZATION of
ELECTRONICS
READOUT
PRACTICAL LIMITATIONS !

SEGMENTATION

CHARACTERISTICS CHARGE
AMPLIFIER

- CHARGE to VOLTAGE GAIN $A \approx \frac{1}{C_f}$

- FEEDBACK $h_{fb} \approx \frac{C_f}{C_d + C_i + C_f}$

- LOAD CAPACITANCE $C_L \approx C_o \approx h_{fb}(C_d + C_f)$

- INTEGRATING
TIME CONSTANT $\tau_a \approx \frac{C_L}{h_{fb} g_m}$

SERIES NOISE DOMINANT -->

ENC² $\approx \frac{kT(C_d + C_i)^2}{g_m}$

SEGMENTATION

SEGMENTATION IN n SEGMENTS
 of SENSOR "DETECTOR"

CAPACITANCE $C_d \approx \frac{C_d}{n} \approx C_s$
 and

ALSO for AMPLIFIER
 C_i, C_f, C_o each / n

READOUT TRANSISTOR
MATCHED with SENSOR CAPACITANCE

IN FIRST APPROXIMATION
TRANSISTOR DOMINATES CHARACTERISTICS
SPEED, NOISE, POWER

SCALING of TRANSISTOR
--> TRANSCONDUCTANCE $g_m \approx \frac{g_m}{n}$
proportional to current I

SEGMENTATION

CHARACTERISTICS CHARGE
AMPLIFIER

- CHARGE to VOLTAGE GAIN $A \approx \frac{1}{C_f} \approx \frac{n}{n}$

- FEEDBACK $h_{fb} \approx \frac{C_f}{C_d + C_i + C_f} \approx 1$

- LOAD CAPACITANCE $C_L \approx C_o \approx h_{fb}(C_d + C_f) \approx n$

- INTEGRATING
TIME CONSTANT $\tau_a \approx \frac{C_L}{h_{fb} g_m} \approx 1$

SERIES NOISE DOMINANT -->

ENC² $\approx \frac{kT(C_d + C_i)^2}{g_m}$

SEGMENTATION

INTEGRAL DETECTOR $\rightarrow C_d$
 SEGMENTED DETECTOR $n \times C_s$

CONSIDER TWO CASES :

1. **CONSTANT POWER** $P_d = n \times P_s$
 CURRENT I SCALED BY n

THEN $ENC_s \ ? \ \frac{ENC_d}{\sqrt{n}}$

2. **CONSTANT NOISE** $ENC_d = ENC_s$

$? P_s = P_d / n$

CURRENTS REDUCED, NOT 'REALISTIC'

SEGMENTATION

PRACTICAL LIMITATIONS

NO SCALING if CAPACITANCE DOMINATED
 by
 CAPACITANCE to NEIGHBOURS and
 PARASITICS

BETTER FOR THINNER SUBSTRATE
 BUMP BOND ($\sim 100\text{fF}$) < WIREBOND ($\sim 1\text{pF}$)

PRACTICAL LIMIT on TRANSISTOR CURRENT
 BUT HIGHER CURRENT RESULTS IN
 LOWER NOISE
 HIGHER SPEED

MATCHING BETWEEN SMALL TRANSISTORS
 and
 SMALL CURRENTS IS REDUCED
 IMPROVES WITH NEWER CMOS
 TECHNOLOGIES

LARGE NUMBER of SEGMENTS LEADS to
 CONNECTIVITY and DATA FLOW PROBLEMS
 INCREASED COMPLEXITY + POWER

is POWER the MAIN LIMITATION ?

EXAMPLE SEGMENTATION

DETECTOR

10 pF, NOISE 2000 e^- rms , power 2 mW
 eg Si diode 10 mm²

SEGMENT IN 1000 SEGMENTS

$\rightarrow 100\mu\text{m} \times 100\mu\text{m}$

1. CONSTANT POWER

\rightarrow POWER per SEGMENT 2 μW

\rightarrow NOISE $\times 1/\sqrt{n}$ 1000 $\sim 63 e^-$ rms

2. CONSTANT NOISE of 2000 e^- rms

\rightarrow POWER per SEGMENT 2 nW (??)

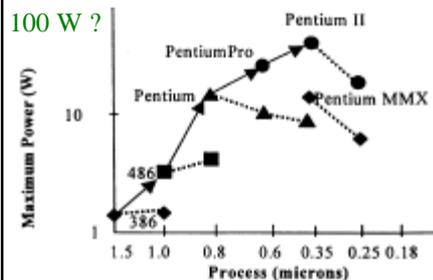
\rightarrow TOTAL POWER 2 μW

TOTAL POWER USUALLY HIGHER

NOISE ACHIEVED 50 - 100 e^- rms

POWER DISSIPATION

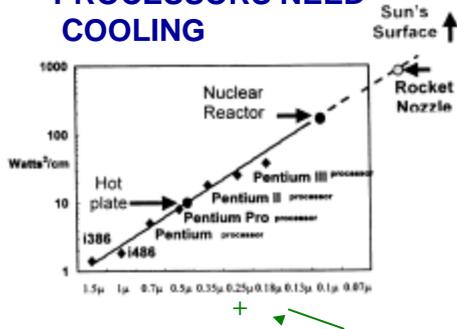
INTEL PROCESSORS RUN HOT



SPEED INCREASE
 MORE FUNCTIONS
 LARGER AREA

OPTIMIZATION in
 NEWER VERSIONS

**POWER DISSIPATION
PROCESSORS NEED
COOLING**



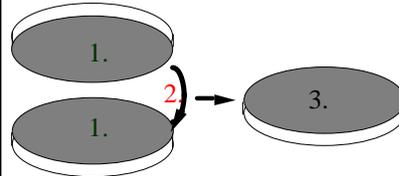
ALICE1 PIXEL CHIP 2.7 cm^2
USES 0.6 to 0.9 W + 0.3 W cm^{-2}

PIXELS vs Si MICROSTRIP
 $\sim 3 \text{ kW m}^{-2}$ vs $0.2 - 0.6 \text{ kW m}^{-2}$

CRYOGENIC OPERATION ?

**'NEW' TECHNOLOGIES
SOI CMOS**

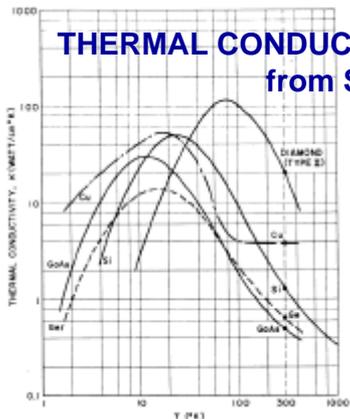
ACTIVE Si on ISOLATING
BURIED OXIDE
VARIOUS WAYS to MAKE SOI



1. OXIDIZED WAFERS
2. FUSE WAFERS
3. LAP-ETCH AWAY MOST of BACK
4. 2-4 μm Si for ACTIVE CMOS

STACK can be made by REPEATED
OXIDATION-BACKLAPPING

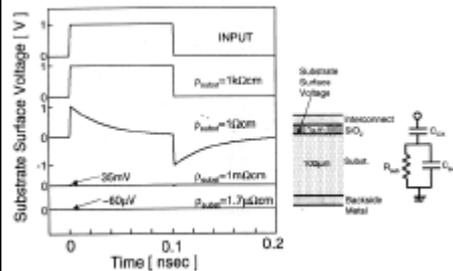
**CRYOGENIC OPERATION
THERMAL CONDUCTIVITY
from Sze**



AT 100K Si $\sim 8 \text{ W / cm K}$
Cu 4 W / cm K
AT 70 Si $\sim 15 \text{ W / cm K}$
Cu 6 W / cm K

NOTE EXCEPTIONAL CONDUCTIVITY
of DIAMOND !

**CROSS TALK in MIXED MODE
BASIC PROBLEM at HIGH FREQ
with SENSITIVE INPUT NODES**



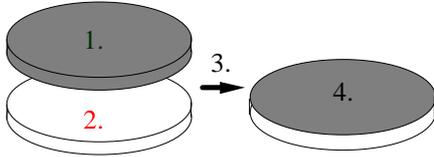
REMEDIES

- low ? SUBSTRATE
- LOW VOLTAGE DIFFERENTIAL
- COAXIAL LINES
- ISOLATING SUBSTRATE (eg SOA)
- OPTICAL TRANSMISSION (on chip)

FOLLOW RF DEVELOPMENTS

3 - D TECHNOLOGIES

Si on Anything : SOA

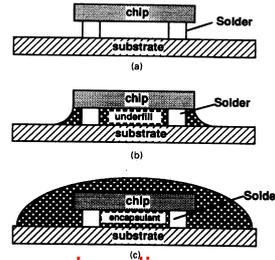


1. SOI wafer with BURIED OXIDE carries bipolar and/or CMOS FACE DOWN
 2. 'ANYTHING' eg GLASS insulating substrate
 3. GLUE TOGETHER
 4. REMOVE Si SUBSTRATE
low parasitics, perfect isolation, low power
- 2.5 GHz for low power RF receiver
(Philips, Proc. IEEE 88(2000) 1546)

INTERCONNECTIONS SENSOR AND READOUT

HYBRID SYSTEM

- FLEXIBILITY IN CHOICE TECHNOLOGY
- NO STANDARDIZATION
- IN FINE PITCH BUMP BONDING
- RELIABLE, STABLE



- bump bonding
- a) bumps only
 - b) underfill
 - c) encapsulation

INTERCONNECTIONS SENSOR AND READOUT

AC COUPLING

- QUALITY, INTEGRATION of CAPACITORS
- MORE SENSITIVE FOR COMMON MODE
- COMPLICATED BIASING
- AVOIDS SHIFT OUTPUT AMPLIFIER

DC COUPLING

- NEEDS STABILISATION OUTPUT POSSIBLE
- NO CAPACITORS, EASIER CONSTRUCTION
- RELIABLE, STABLE

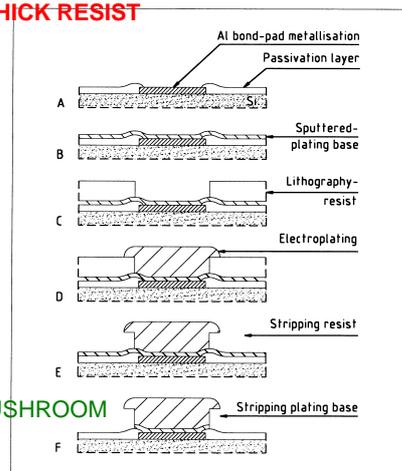
Interconnections

- wire bonding
extensive infrastructure
experience
- bump bonding
small capacitance

INTERCONNECTIONS

BUMP BONDING

- VARIOUS SOLDERS
- ELECTROPLATING
- THICK RESIST

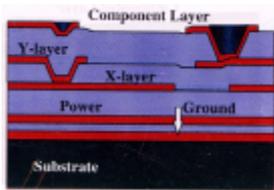


MUSHROOM

PACKAGING TECHNOLOGIES
can be used in **PARTICLE**
PHYSICS

HYBRIDIZATION using
SENSOR as **SUBSTRATE**
SPECIAL CONSTRAINTS
THIN, 'LOW MASS' ASSEMBLY POSSIBLE

MCM - D
Multi Chip Module DEPOSITED
on **CERAMIC**
on **Si**



IMEC
Leuven

SILICON AS MECHANICAL
SUPPORT

SILICON MICROMECHANICS

AVAILABILITY
FLATNESS at μm LEVEL
FAIRLY LARGE AREA
EXTENSIVE R&D GOING ON
COOLING CHANNELS INSIDE

GOOD FOR PHYSICS
FAIRLY LOW Z

PACKAGING TECHNOLOGIES
Multi Chip Module
'SIMPLE' MCM on Si



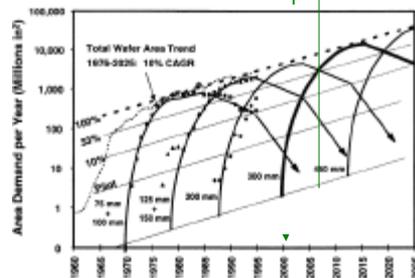
SENSOR CARRIES 16 CHIPS

BUMP BONDING on **SENSOR**

1996 DELPHI pixel

Si WAFER SIZE

300 mm HAS JUST STARTED



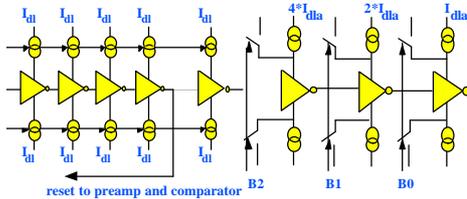
FACTORY INVESTMENT >> B\$

NEW CMOS LINKED TO LARGE
WAFERS / LARGE VOLUME

SPECIAL HARDWARE & LOGISTICS
for SMALL VOLUME ORDERS
CAN BACK-END PROCESSING FOLLOW ?

PARAMETER ADJUSTMENT

LHC1 CHIP: DELAY LINE IN PIXEL



CURRENT STARVED INVERTER ARRAYS

36 INVERTER STAGES

I_{d1} CAN BE TUNED 40 - 100 μA \rightarrow 3.5 - 1.5 μs

3 INVERTER STAGES for DIGITAL TRIM

I_{d1a} CAN BE SET TO RANGE

60 ns - 300 ns FOR EACH STEP

PROVIDE ADJUSTABLE RANGE
ALSO TO THE STEP VALUE



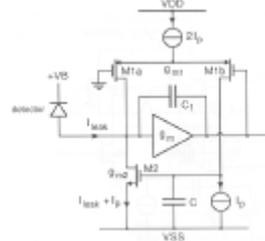
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LEAKAGE CURRENT COMPENSATION

LOCAL ANALOG ADJUSTMENT
USING ACTIVE FEEDBACK



F. Krummenacher NIM A305(1991) 527

Equivalent Feedback Resistor $R_f \approx 1 / g_{m1}$

Detector Leakage Current flows into M2

I_{leak} can be much larger than I_p

PIXELS \sim 200 nA

\sim nA



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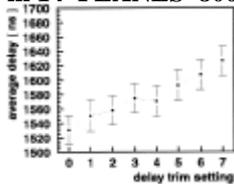
PARAMETER ADJUSTMENT

DIGITAL DELAY TRIM

RD19/LHC1 PIXEL DETECTOR

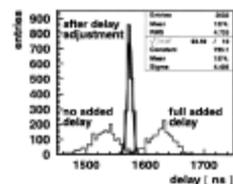
UNIFORMITY for STROBE

in 14 PLANES 800 CHIPS, 400 cm^2



8 SETTINGS (3 bits)
1530 ns - 1630 ns

ALSO OVERALL RANGE
CAN BE TUNED



on single chip 6 ns rms

1 plane 48 k cells
80 ns \rightarrow 16 ns rms

E. Cantatore et al. NIM A409(1998) 119



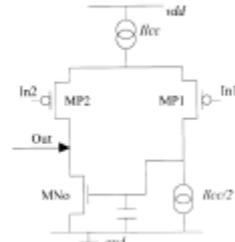
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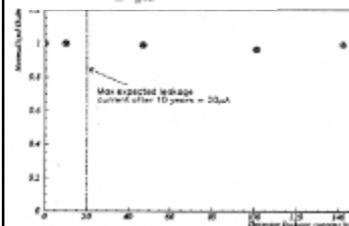
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LEAKAGE CURRENT COMPENSATION

'DELTA' Si DETECTOR AMPLIFIER



P. Aspell et al.
For CMS
Preshower



CURRENT COMPENSATED up to 150 μA

COMPENSATION USES ONLY 5 μW



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SYSTEM MANAGEMENT

VARIETY of FUNCTIONS
MAY BE IMPLEMENTED on
SENSOR READOUT CHIPS

POWER DISTRIBUTION

LASER DRIVEN POSITIONING

TEMPERATURE SENSOR

MAGNETIC FIELD SENSOR ?

OTHERS ???

CMOS COMPATIBILITY NOT GRANTED



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3 - D TECHNOLOGIES

DEVELOPMENT of 3 - D
is INSPIRED by
NEED for MORE DENSITY

CAN IT BE USED for PHYSICS ?

MORE ELECTRONIC FUNCTIONS
per UNIT of AREA

MULTIPLE DETECTION LAYERS
'TRACK VECTOR
DETECTORS'

OTHER ??



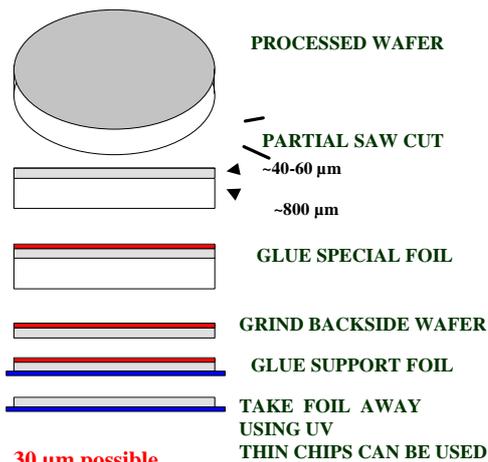
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THIN DEVICES

DBG : Dice Before Grind



TOSHIBA + DISCO + LINTEC



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CONCLUSION

CHIP TECHNOLOGY -> NEW DETS

SINGLE QUANTUM PROCESSING

MHz OPERATIONS IN PIXEL
eg counting at 10^{11} cm^{-2}

FOLLOW INDUSTRY TRENDS

NEW PHYSICS, IF IT IS THERE



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