

CMOS Pixels for Particle Tracking

By: Grzegorz DEPTUCH

IReS/LEPSI, IN2P3/ULP, 23, rue du Loess BP20, F-67037 Strasbourg, France
UMM, al. A. Mickiewicza 30, 30-059 Krakow, Poland

Contents

- Short history of monolithic pixels
- Idea and basic architecture
- Why pixels CMOS?
- Simulations of physics process
- Prototype MIMOSA chips
- Readout and data processing - now
- Calibration of the conversion gain
- Charge collection time
- Radiation hardness (?)
- Tracking results
- Prospects
- Conclusions



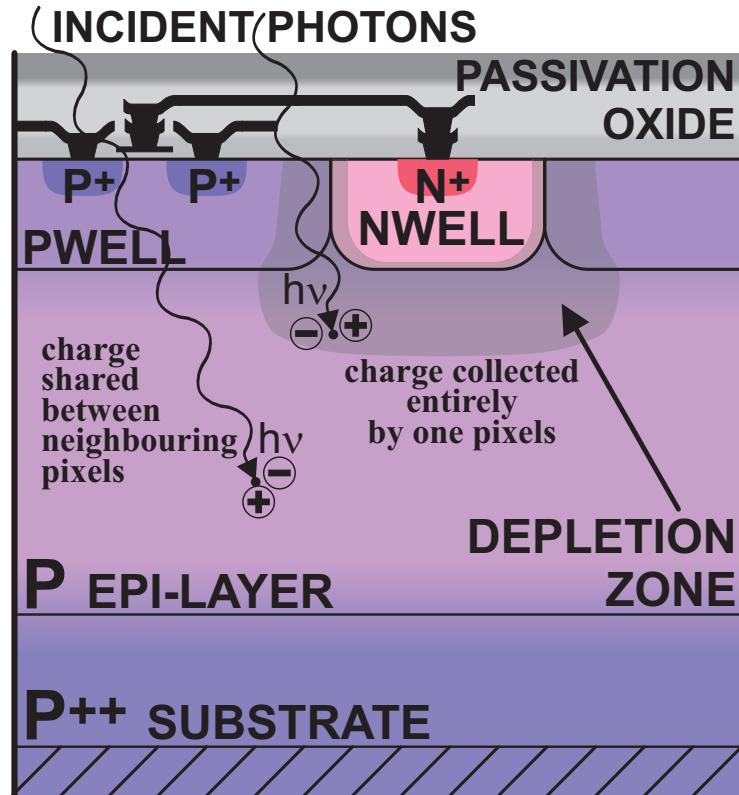
Short history of monolithic pixels

- 1987-1994 University of Hawaii,**
VLSI pixel device for particle detection
p-type high resistive silicon substrate, detector - PDIFP-PSUB/NDIFF diode, electronics - PMOS transistors in NWELL, CMOS at the periphery
- 1993-1996 CERN,**
monolithic silicon pixel detectors in SOI technology
n-type high resistive silicon substrate SOI, detector - PDIFP/NSUB, electronics - CMOS SOI
- 1994-1997 KEK National Laboratory for High Energy Physics,**
pMOS pixels
p-type high resistive silicon substrate, detector - PMOS transistor in floating NWELL, electronics - CMOS at the periphery
- 1998-... IReS/LEPSI,**
pixels CMOS
p-type low resistive epitaxial substrate, detector - NWELL/PSUB diode, electronics - NMOS transistor in NWELL, CMOS at the periphery
1999 - first small scale prototypes
1999-2000 first beam tests ($\sigma \sim 1.5 \mu\text{m}$, $\epsilon \sim 99\%$)
2001 - expect first large scale prototype



Idea and basic architecture

- ◆ from digital still and video cameras

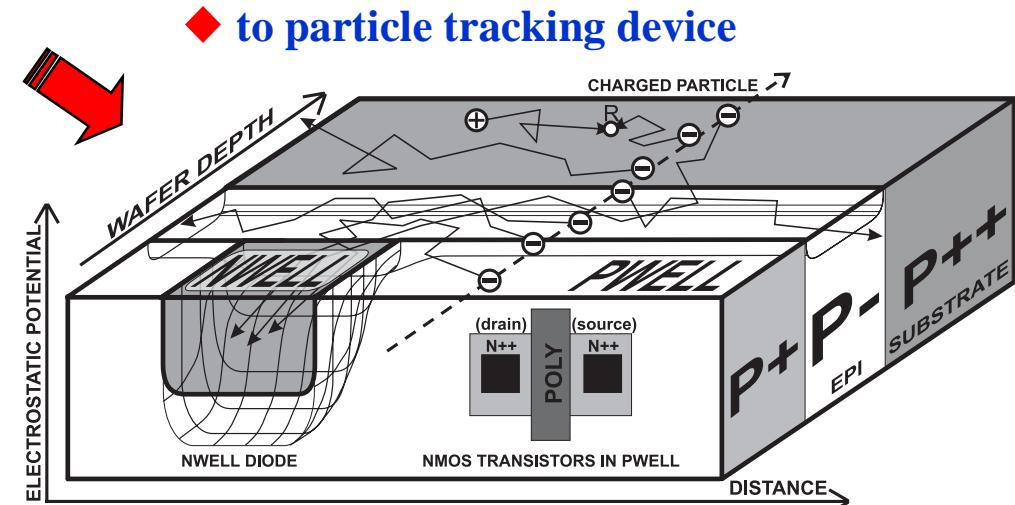


Twin - tub (double well), CMOS process with epitaxial layer

The ‘warmest’ colour represents the highest potential in the device



Katedra Elektroniki
AGH, Krakow



- The effective charge collection is achieved through the thermal diffusion mechanism,
- The device can be fabricated using a standard, cost-effective and easily available CMOS process,
- The charge generated by the impinging particle is collected by the n-well/p-epi diode, created by the floating n-well implantation,
- The active volume is underneath the readout electronics allowing a 100% fill factor, as required in tracking applications.

- operation ‘in the dark’
- only sporadic hits
- very low signals

Why CMOS?

- Why monolithic pixel devices:
 - 1 unique substrate for detector and electronics:
 - thin device \Rightarrow reduced multiple scattering effect,
 - no detector-electronics connection (neither complicated and expensive bump- nor fragile wire- bonding).

Why pixels CMOS:

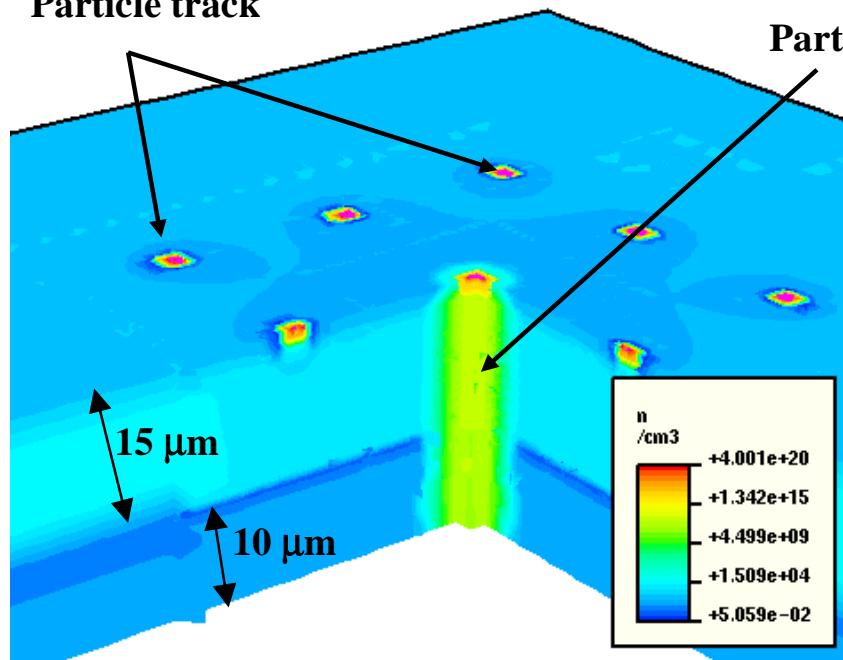
- standard, well established industrial fabrication process:
 - access to the most advanced technologies - no expensive own development,
 - convenient way of design - standard software tools, design kits and libraries,
 - good price and high yield !
 - low power consumption,
- CMOS process:
 - system-on-a-chip capability - integration of amplifiers, ADCs, signal processing units etc. on the detector, random pixel addressing,
 - detector radiation hardness - no bulk charge transfer (CCDs).
- submicronic CMOS:
 - very good spatial resolution ($\sim 1 \mu\text{m}$) - small pixel size,
 - electronics radiation hardness (layout rules).



Katedra Elektroniki
AGH, Krakow

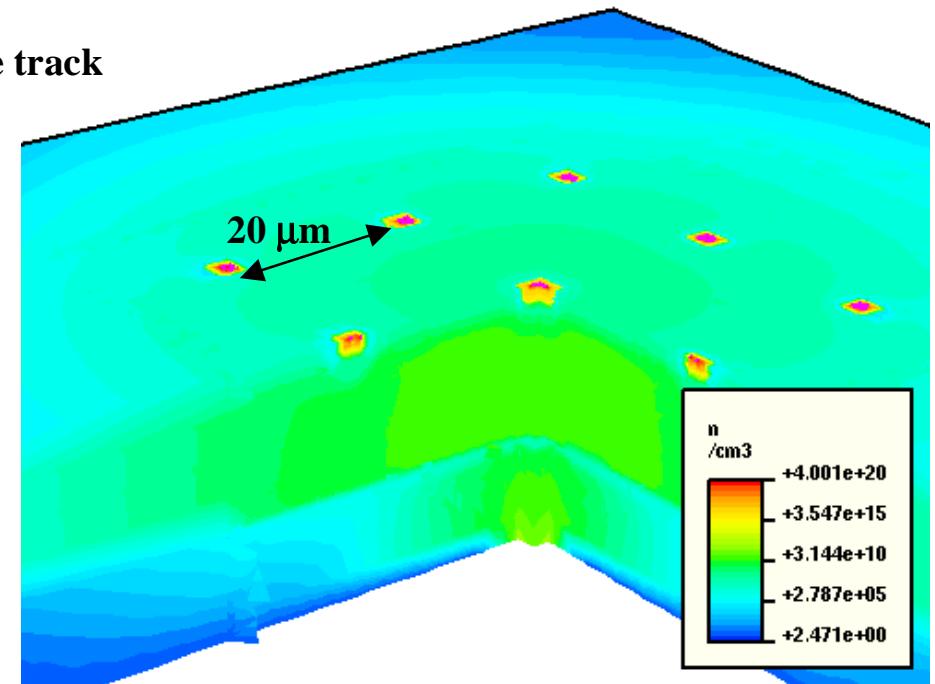
Simulation of physics process

Particle track



$\tau = 0 \text{ ns}$

Particle track



Carrier concentration

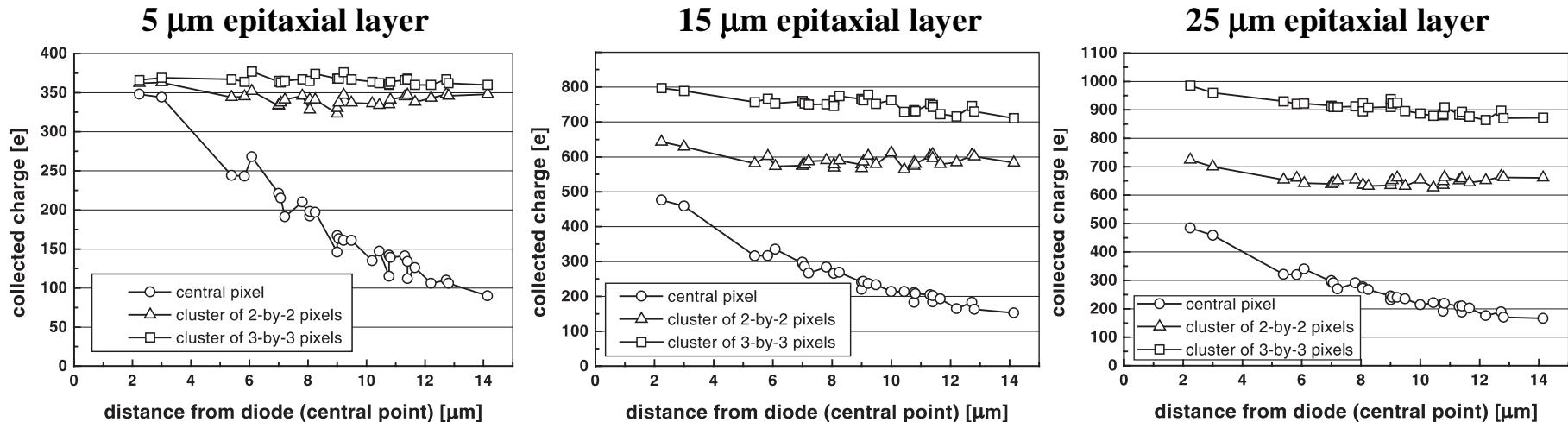
$\tau = 25 \text{ ns}$

- The charge collection efficiency examined using the mixed mode device and circuit simulator DESSIS-ISE from the ISE-TCAD package,
- The charge collection is traced as a relaxation process of achieving the equilibrium state after introducing an excess charge emulating passage of the ionising particle
- The device is described in three dimensions by a mesh generated using the analytical description of doping profiles and the boundary definition corresponding to the real device,
- Different detector parameters, including the thickness of the epitaxial layer, the size of a pixel and collecting diodes and number of diodes per pixel, were investigated.

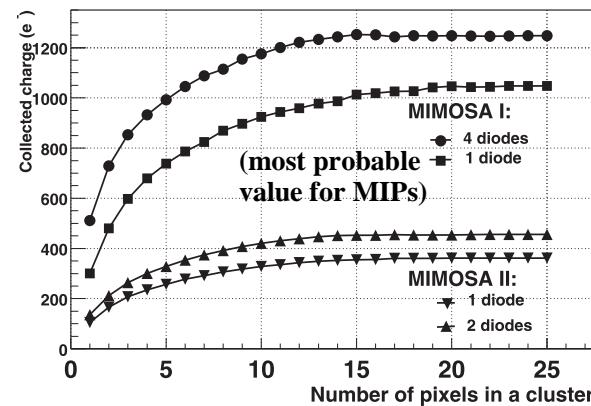


Simulation of physics process

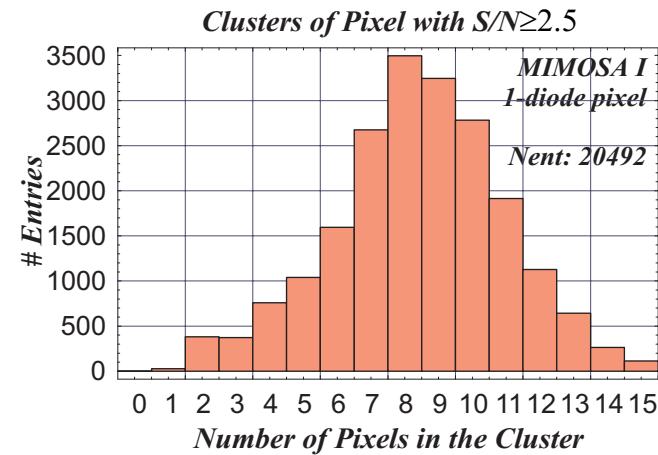
- Simulation of charge collection:



- Experimental verification:



The measured collected charge for two chips having 14 μm and less than 5 μm, the pitch of 20 μm



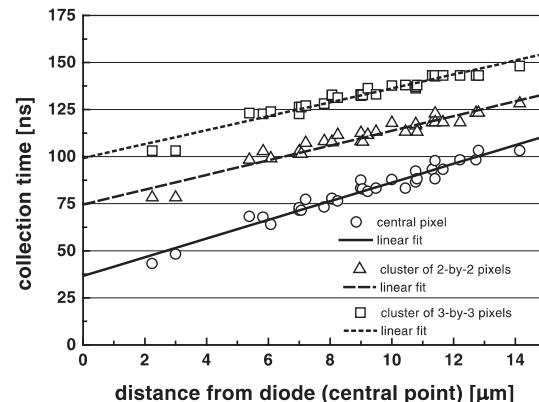
for the chip with 14 μm of the epitaxial layer



Katedra Elektroniki
AGH, Krakow

Simulation of physics process

- Simulation of charge collection time:

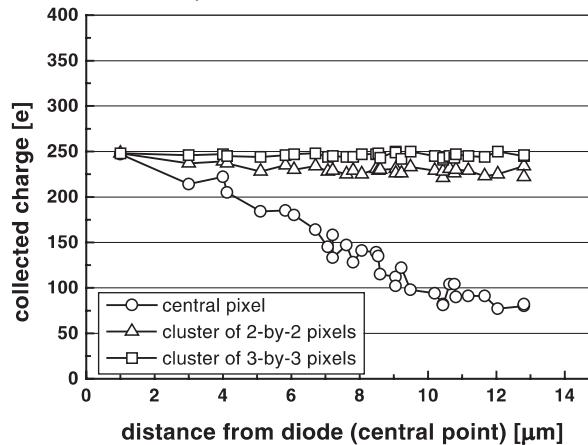


15 μm epitaxial layer

Charge collection time
(90 % of charge)
<150 ns

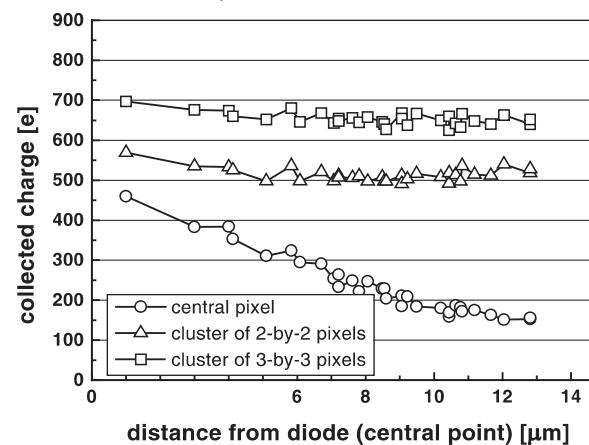
- Highly doped substrate contribution:

5 μm epitaxial layer



$$370e^- \Rightarrow 250e^- (\sim 32\%)$$

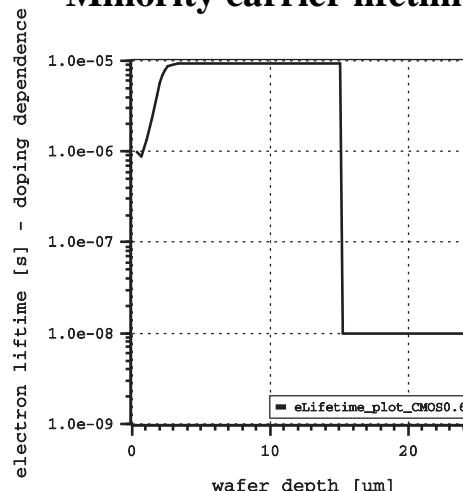
15 μm epitaxial layer



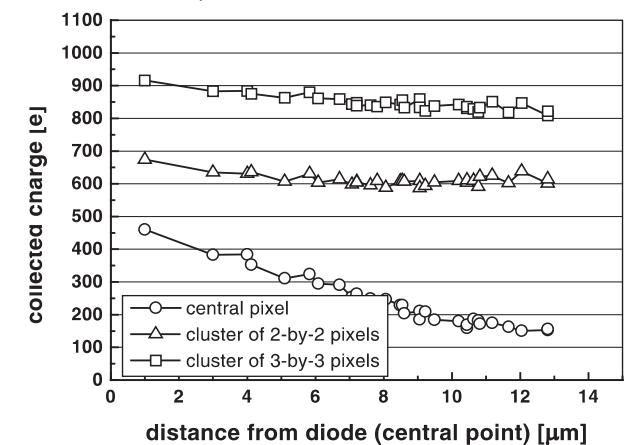
$$780e^- \Rightarrow 670e^- (\sim 14\%)$$

Simulations supposing substrate thickness = 0 μm

Minority carrier lifetime



25 μm epitaxial layer



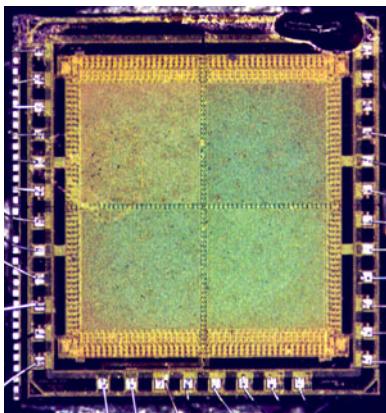
$$920e^- \Rightarrow 860e^- (\sim 6\%)$$



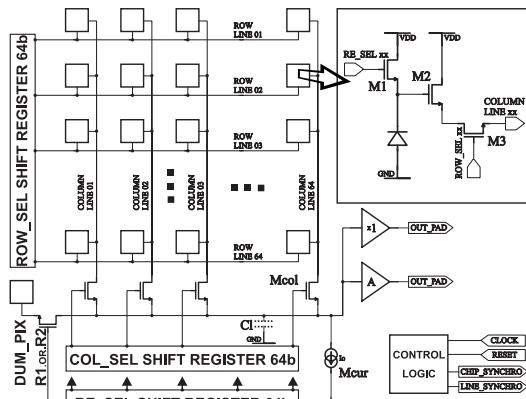
Katedra Elektroniki
AGH, Krakow



Prototype MIMOSA chips



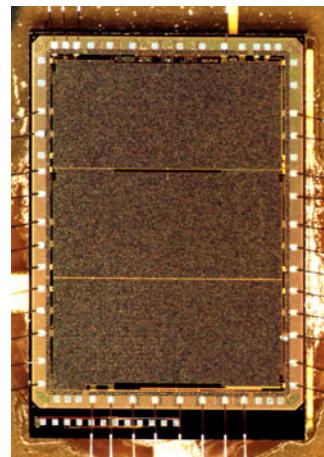
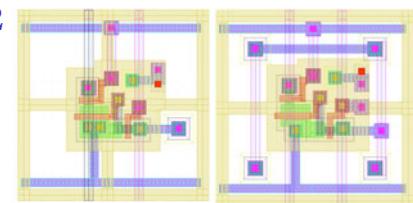
MIMOSA I die photo



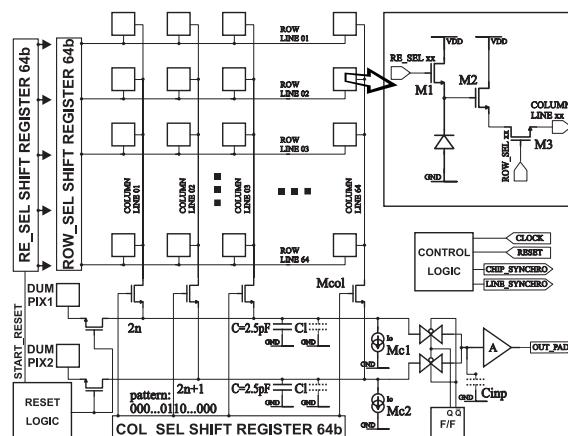
MIMOSA I block schematic diagram

- standard $0.6\mu\text{m}$ CMOS ($\text{tox}=12.7\text{nm}$)
- $14\mu\text{m}$ thick EPI layer (10^{14}cm^{-3})
- 4 arrays 64×64 pixels
- pixel pitch $20\times 20\mu\text{m}^2$
- diode (nwell/p-epi) size $3\times 3\mu\text{m}^2$ - 3.1fF
- serial analogue readout
- max. clock freq.: 5MHz
- die size $3.6\times 4.2\text{mm}^2$
- technology 3M+2P
- power supply 5V

MIMOSA I
pixels layouts



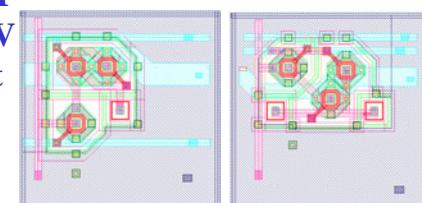
MIMOSA II die photo



MIMOSA II block schematic diagram

- standard $0.35\mu\text{m}$ CMOS ($\text{tox}=7.4\text{nm}$)
- $4.2\mu\text{m}$ thick EPI layer (10^{15}cm^{-3})
- 6 arrays 64×64 pixels
- pixel pitch $20\times 20\mu\text{m}^2$
- diode (nwell/p-epi) size $1.7\times 1.7\mu\text{m}^2$ - 1.65fF
- serial analogue readout
- max. clock freq.: 25MHz
- die size $4.9\times 3.5\text{mm}^2$
- technology 5M+2P
- power supply 3.3V
- radiation tolerant
- transistor design

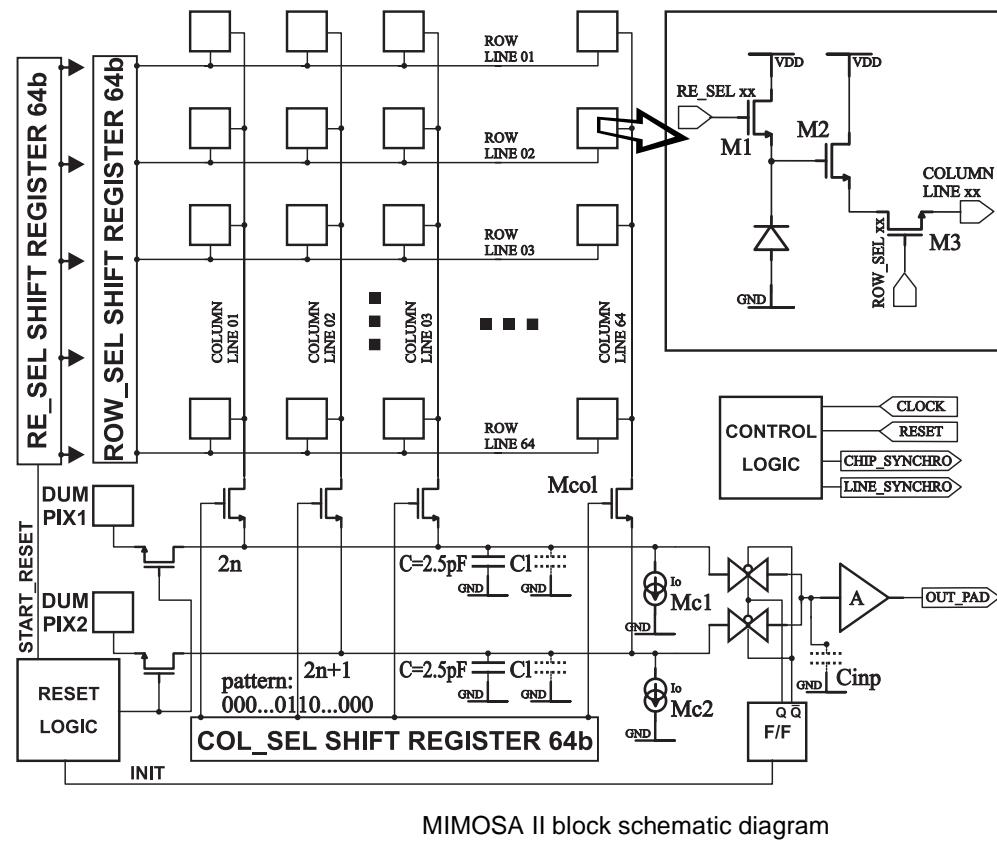
MIMOSA II
pixels layouts



Katedra Elektroniki
AGH, Krakow

MIMOSA - Minimum Ionising Particles MOS APS

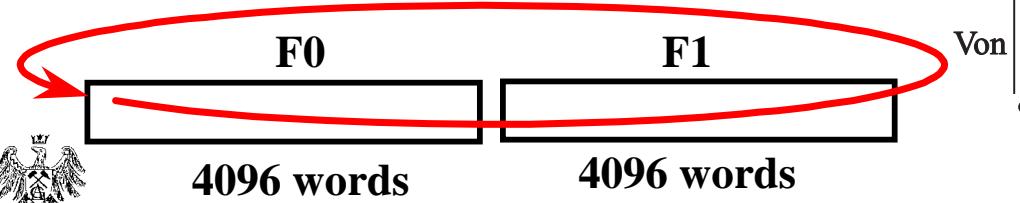
Readout and data processing - now



MIMOSA II block schematic diagram

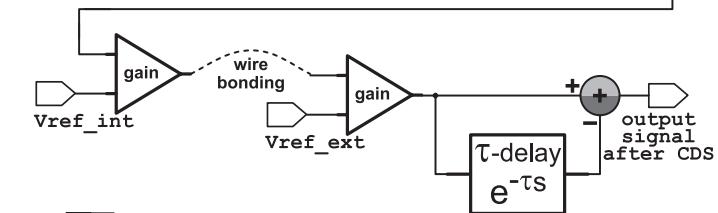
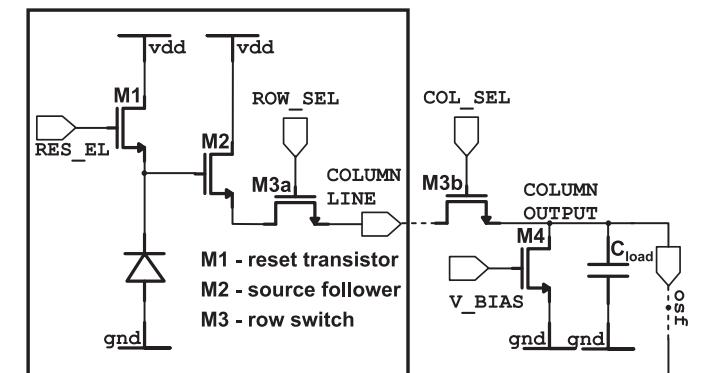
FADC 12 bits

Buffer : 8192 words/channel



Katedra Elektroniki
AGH, Krakow

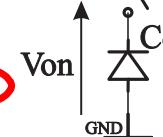
Single pixel architecture with simplified readout and signal processing



kTC noise suppressing

$$\sigma_{V_{on}}^2 = \frac{1}{2\pi} \int_{-\infty}^{+\infty} |H(\omega)|^2 S_{Vn}(\omega) d\omega = \frac{kT}{C_d}$$

Noise kTC [V²]
RON



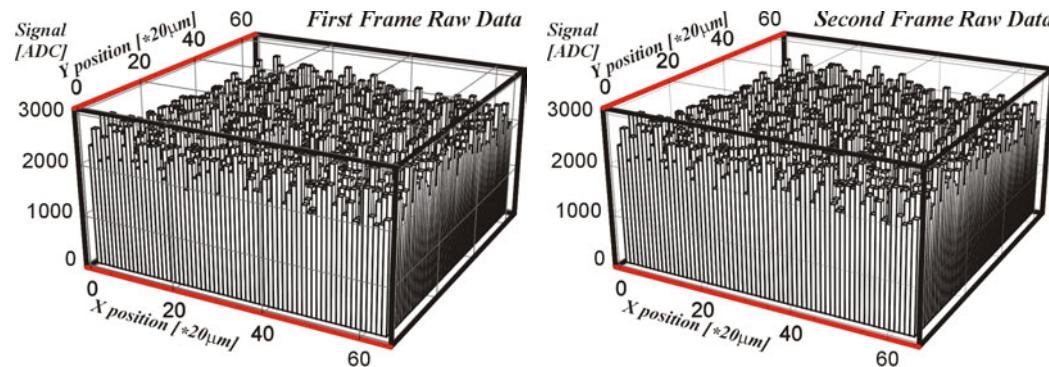
CDS transfer function

$$|H_{CDS}(f)|^2 = \frac{4f_{3dB}^2 \sin^2(\pi f)}{f^2 + f_{3dB}^2}$$

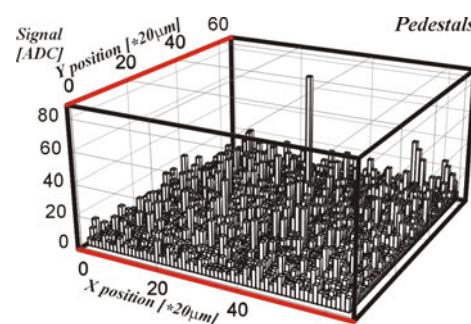


Readout and data processing - now

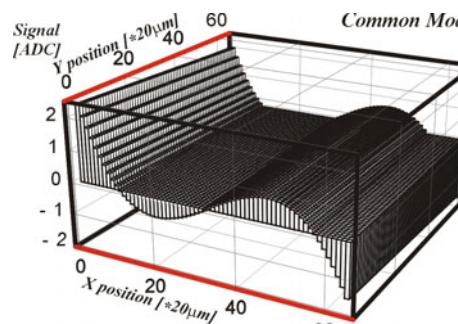
- Off-line CDS:



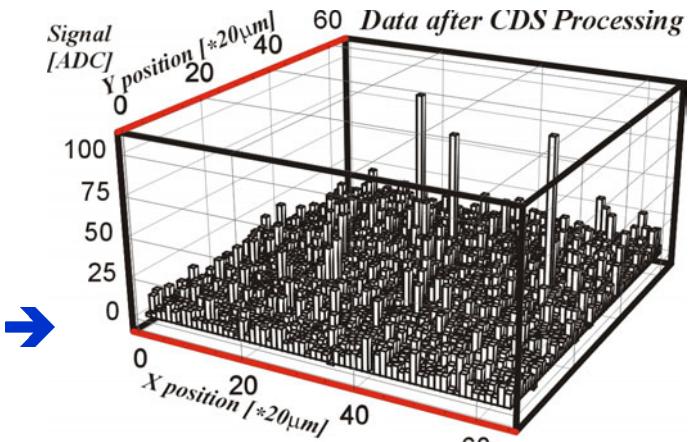
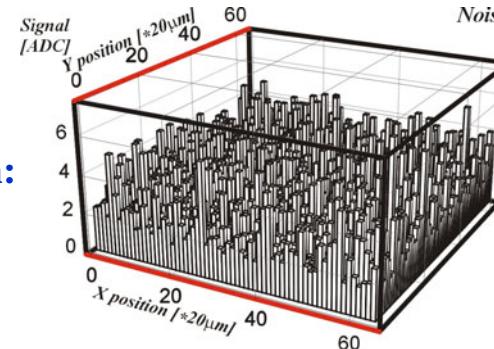
- Pedestals:



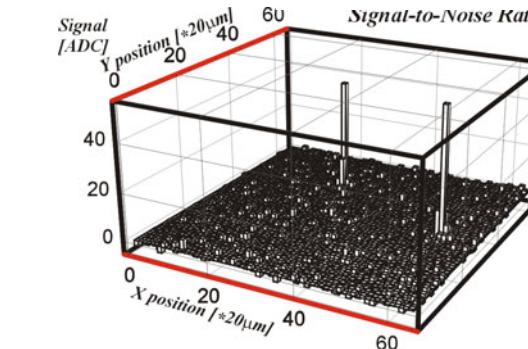
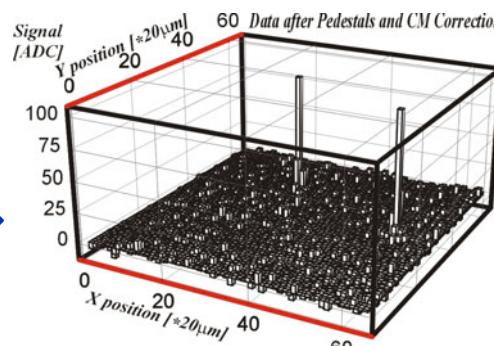
- Common Mode:



- Temporal noise distribution:



frame2 – frame1

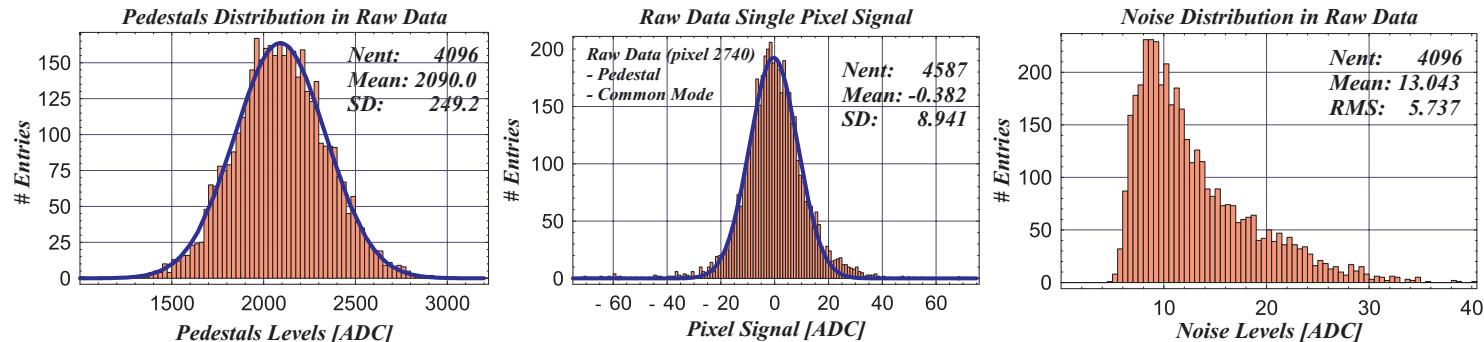


- Signal-to-noise ratio evaluated for considered event

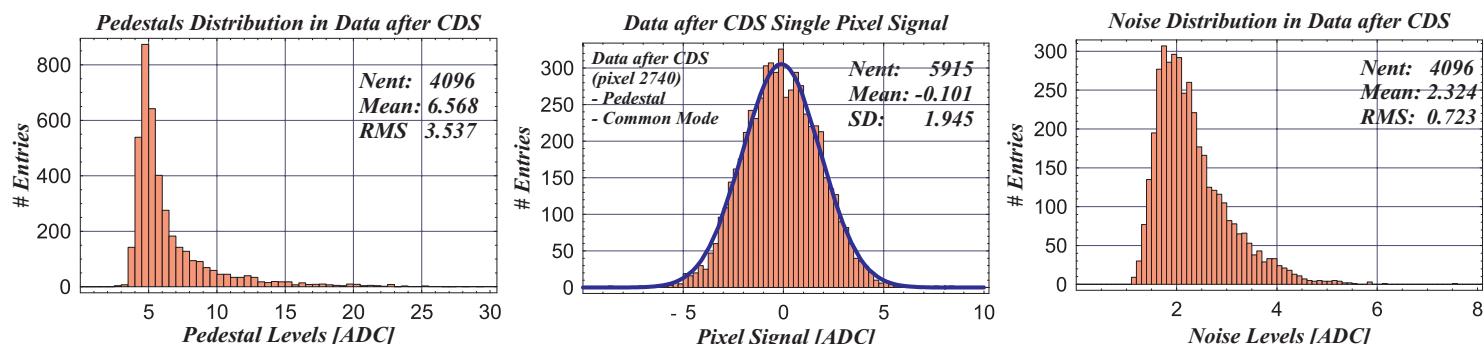


Readout and data processing - now

- Raw data before CDS for MIMOSA I @ -20°C:



- Data after CDS for MIMOSA I @ -20°C:



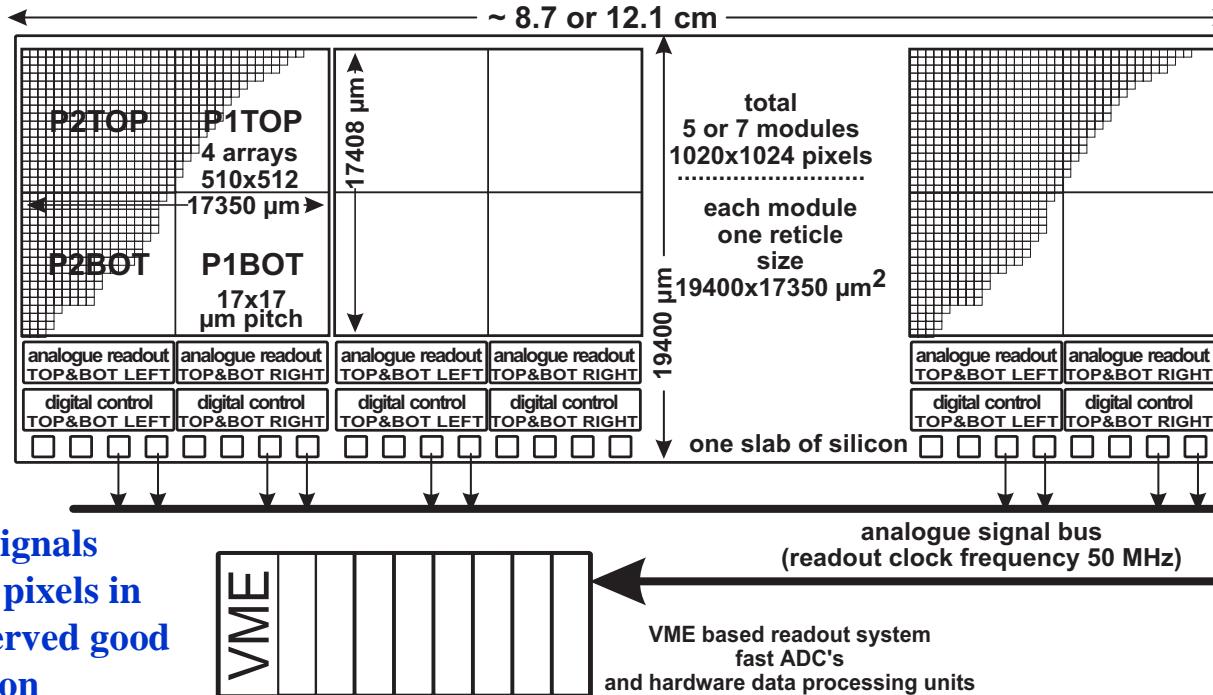
- Summary of measurements (beam tests 120 GeV π):

Collected charge [e-] ‘Landau peak’:		
	seed pixel	3x3 cluster
MIMOSA 1:	1 diode	302 896
	4 diodes	517 1155
MIMOSA2:	1 diode	110 315
	2 diodes	136 407

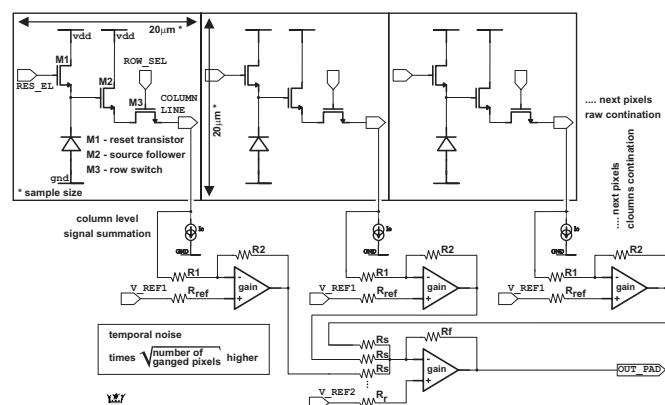
Noise mean [e-]: mean S/N:		
	single pixel	3x3 cluster
MIMOSA 1:	1 diode	12-14 42
	4 diodes	25-30 32
MIMOSA2:	1 diode	9-12 22



Readout and data processing - big chip simple quick start solution



- summing of signals from adjacent pixels in one row - preserved good charge collection



- stitching: coarse - 100 μm , precise - 1 μm
- for larger pitch in one direction - signal summing
- analogue readout - with hardware processing
- process 0.6 μm with 14 μm epitaxial layer
- lot of six 6" wafers 36k



Katedra Elektroniki
AGH, Krakow

Calibration of the conversion gain - with soft X-rays

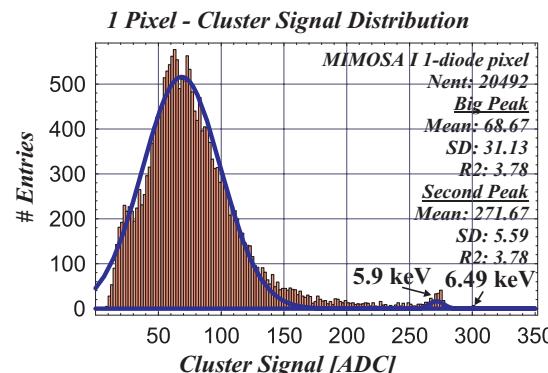
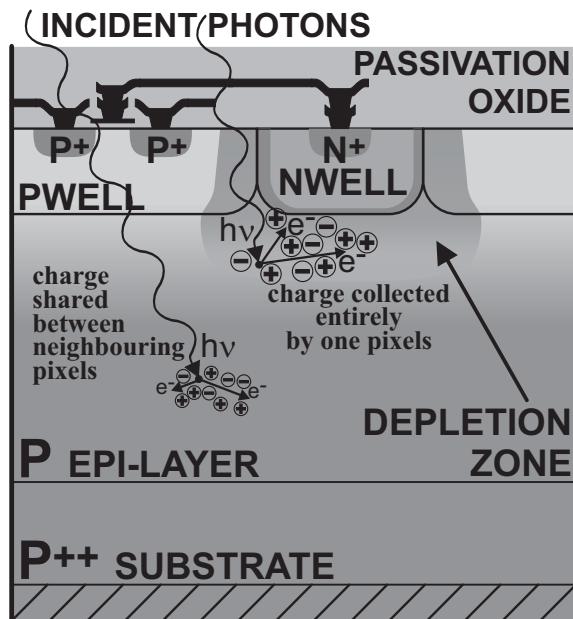
- Calibration methods:

Poisson statistics of the integrated shot noise

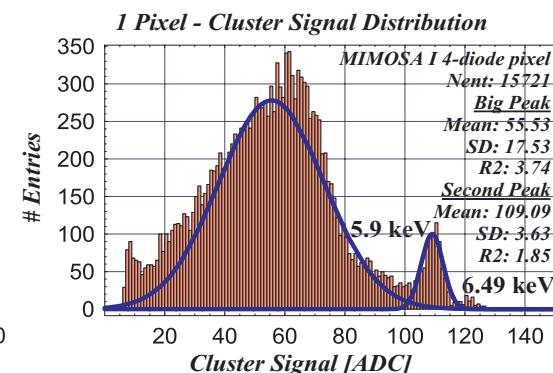
transfer curve of the squared pixel noise upon the measured average signal over certain number of acquired images

Emission spectra of a low energy X-ray source
e.g. iron ^{55}Fe emitting 5.9 keV photons.

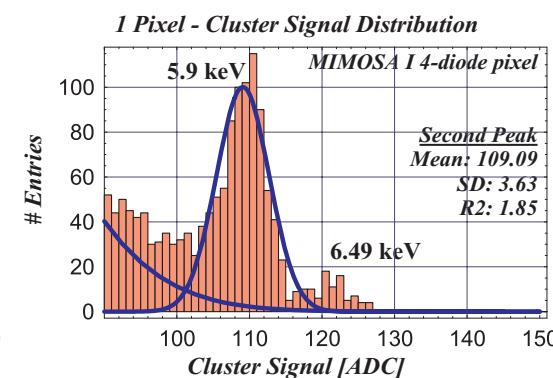
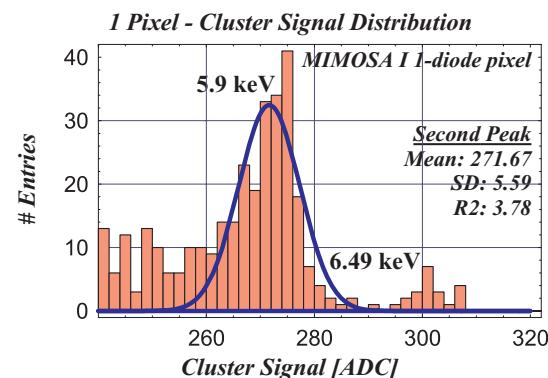
very high detection efficiency even for thin detection volumes - $\mu = 140 \text{ cm}^2/\text{g}$, constant number of charge carriers about 1640 e/h pairs per one 5.9 keV photon



MIMOSA I (14 μm EPI)
configuration with
single diode in one pixel



MIMOSA I (14 μm EPI)
configuration with
four diodes in one pixel



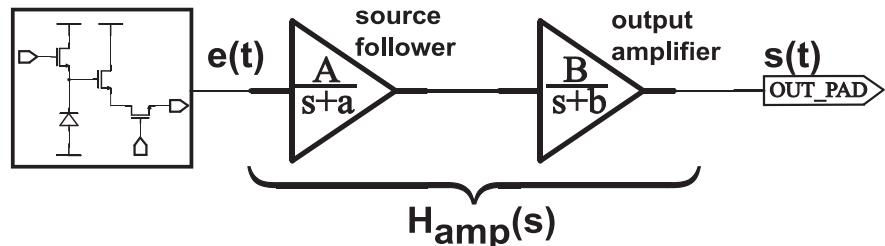
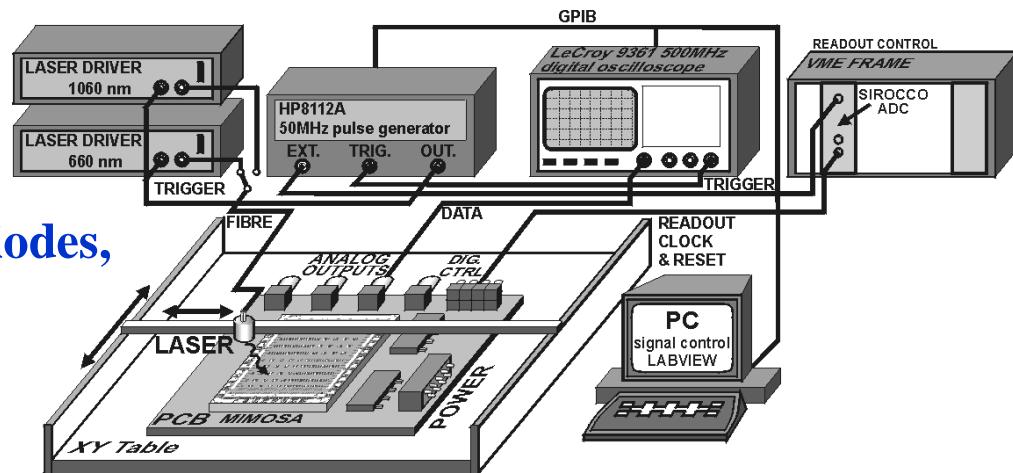
MIMOSA I CMOS 0.6 μm	1 diode – 14.6 $\mu\text{V/e}^-$ ENC = 14 e^- @ 1.6 ms f. rate	4 diode – 6.0 $\mu\text{V/e}^-$ ENC = 30 e^- @ 1.6 ms f. rate
MIMOSA II CMOS 0.35 μm	1 diode rad. tol.– 22.9 $\mu\text{V/e}^-$ ENC = 12 e^- @ 0.8 ms f. rate	2 diode rad. tol.– 17.5 $\mu\text{V/e}^-$ ENC = 14 e^- @ 0.8 ms f. rate



Charge collection time

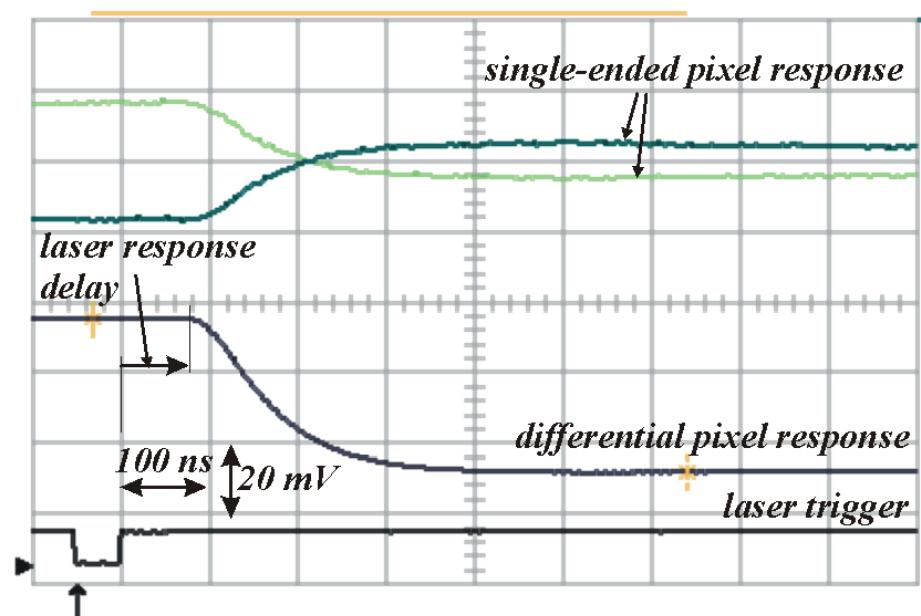
■ Laser test set-up for strip detectors evaluation:

- 660 nm and 1060 nm pulse laser diodes,
- rise time = 0.2 ns,
- pulse width = 8.5 ns,
- spot size 10 μm (FWHM).



$$e(t) = \frac{1}{A \cdot B} \left[\frac{d^2 s(t)}{dt^2} + (a+b) \frac{ds(t)}{dt} + a \cdot b \cdot s(t) \right]$$

- Simple deconvolution results in 100 - 150 ns of charge collection time



Katedra Elektroniki
AGH, Krakow

Radiation hardness (?)

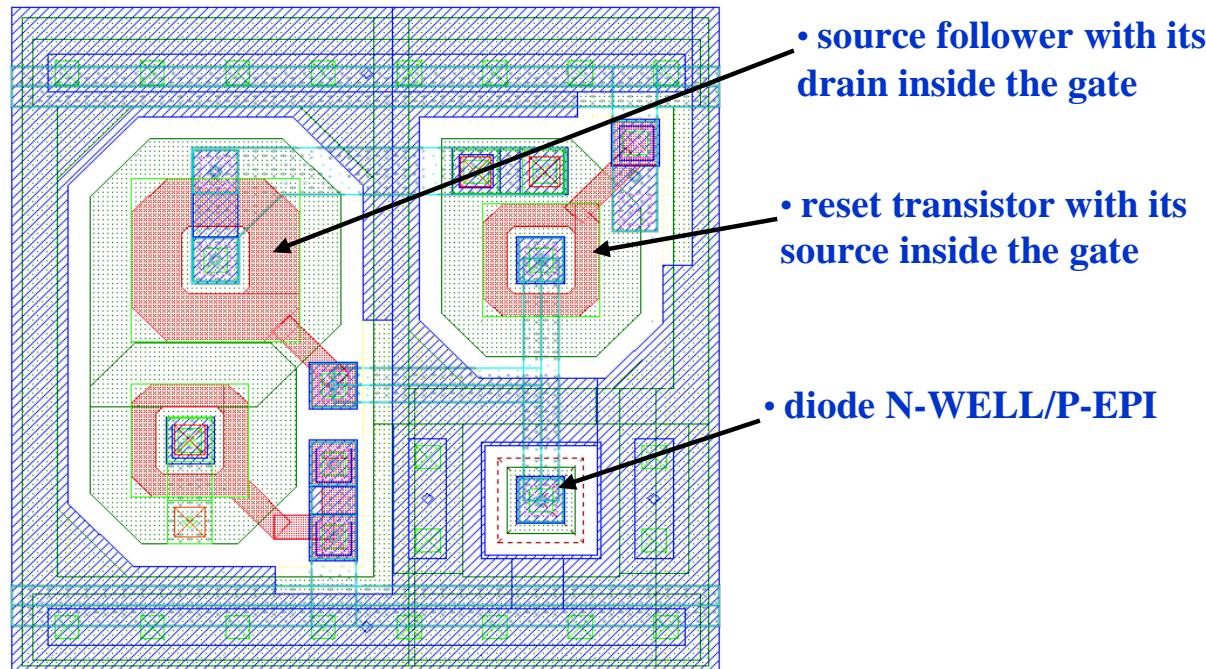
- Pixel layout - radiation tolerant design rules

radiation effects:

- Bulk damages due to mass particles (neutrons, protons and other hadrons) -

carrier lifetime Δt -> faster recombination -> less collected charge

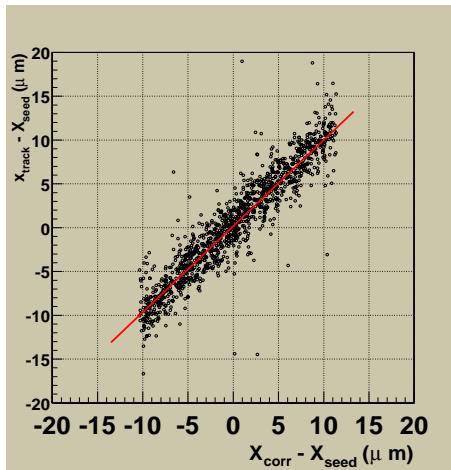
- Positive charge built-up in the oxide close to the silicon interface -> charge losses due to leakage currents and problems in electronics



Enclosed NMOS transistors -> $8 \times 8 \mu\text{m}^2$ in $0.25 \mu\text{m}$ process

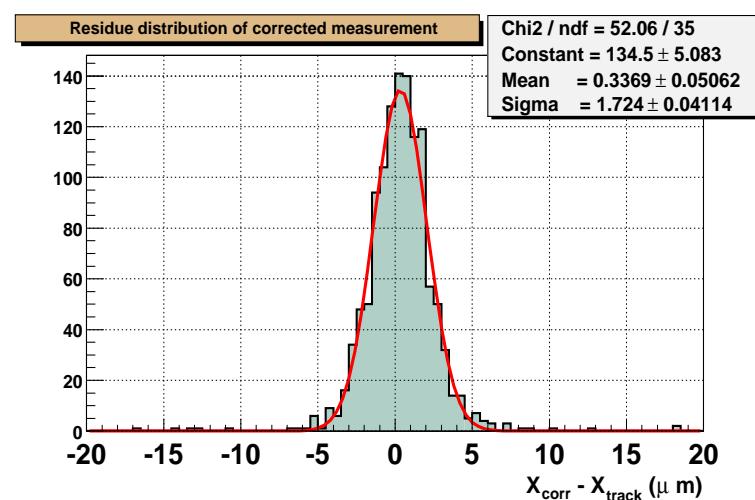
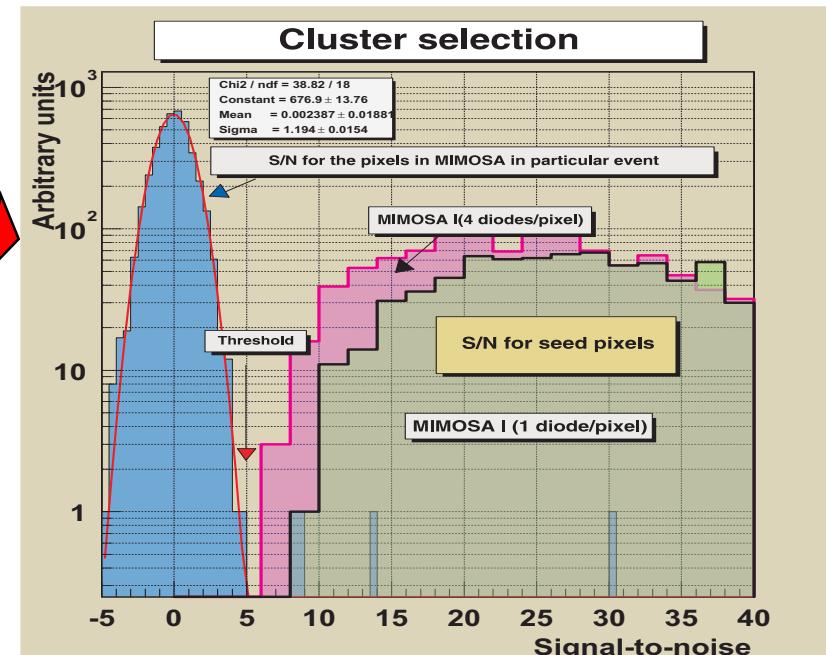


Tracking performance



The high S/N made the pattern recognition easy, clusters selected using the pixels with S/N>5 as a seed ...

The clusters found in MIMOSA matched the track known from the reference detectors' planes ...



CoG with correction

Efficiency (%)

MIMOSA I: 1 diode **99.5 +/- 0.2**
MIMOSA I: 4 diodes **99.2 +/- 0.2**
MIMOSA II: 1 diode **98.5 +/- 0.3**

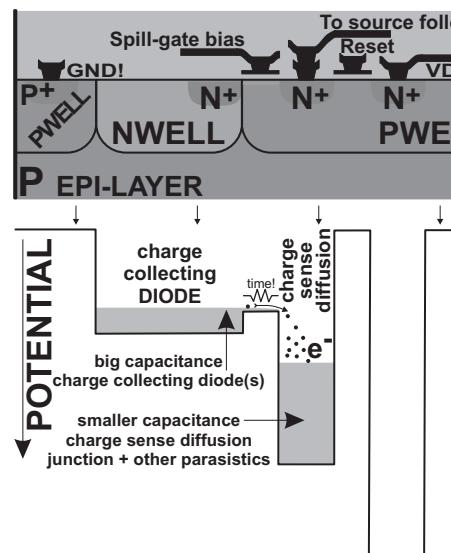
Spatial resolution (μm):

MIMOSA I: 1 diode **1.4 +/- 0.1**
4 diodes **2.1 +/- 0.1**
MIMOSA II: 1 diode **2.2 +/- 0.1**



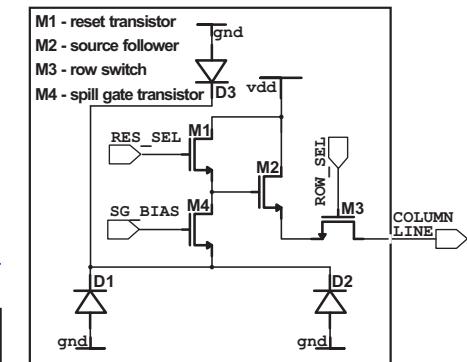
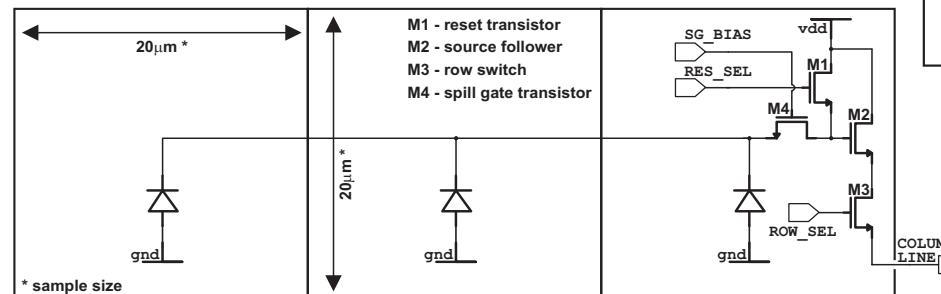
Future prospects

- How to balance good charge collection efficiency and larger pitch (less data)?
 - pixel signal summing on the ganged columns \Rightarrow noise \nwarrow , complexity \nwarrow
 - using spill gate device \Rightarrow speed \nwarrow



• pixels in one row
connected in groups
decreasing effective pitch in
one direction

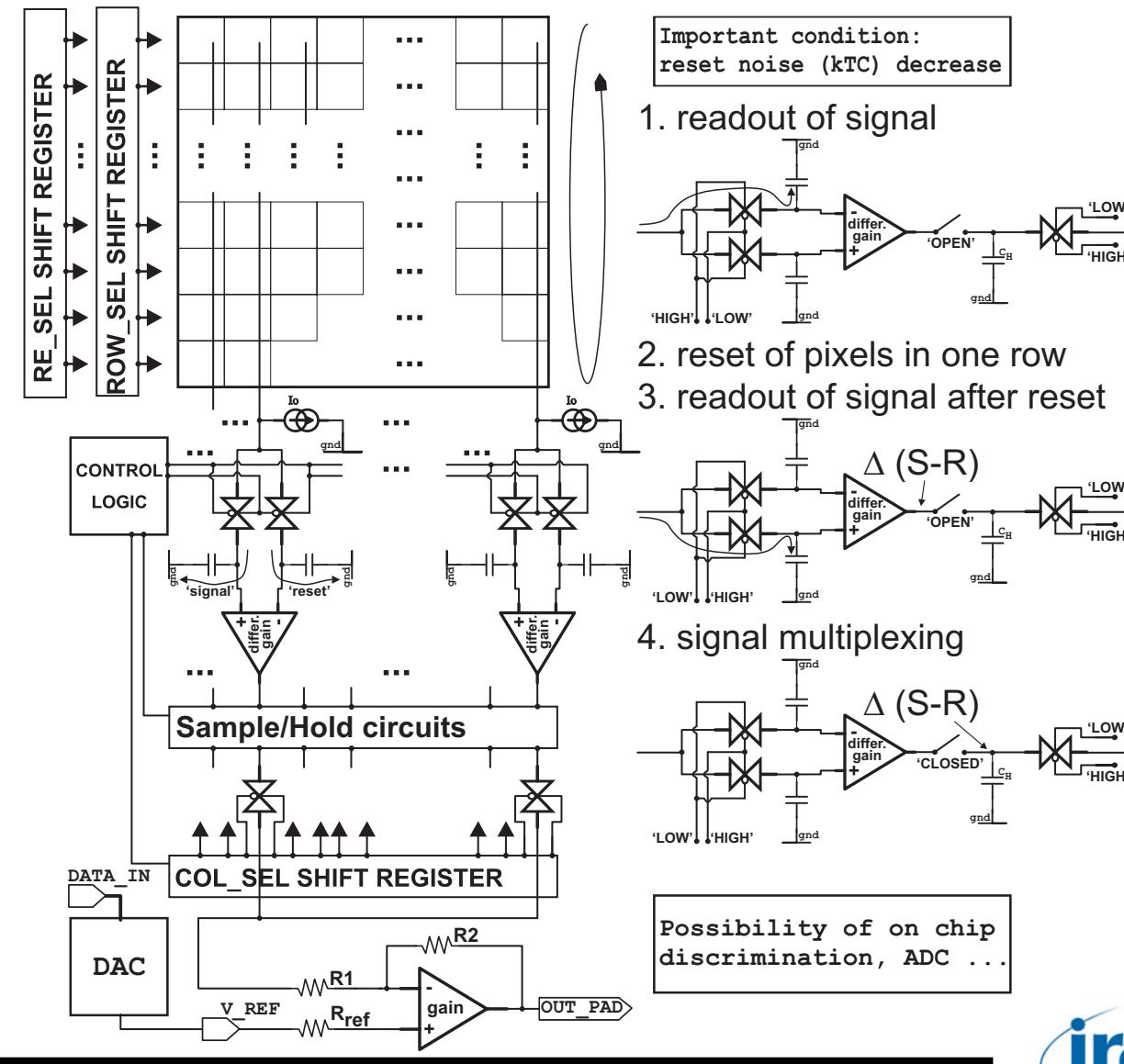
... OR



- How to decrease amount of transferred data and increase speed...
translating to reducing kTC noise and FPN (1st step) \Rightarrow discrimination
and signal processing on chip, and parallel readout
 - CDS on pixel level - not easy - still FPN on column level,
 - using 'active reset method' and DDS parallel column processing

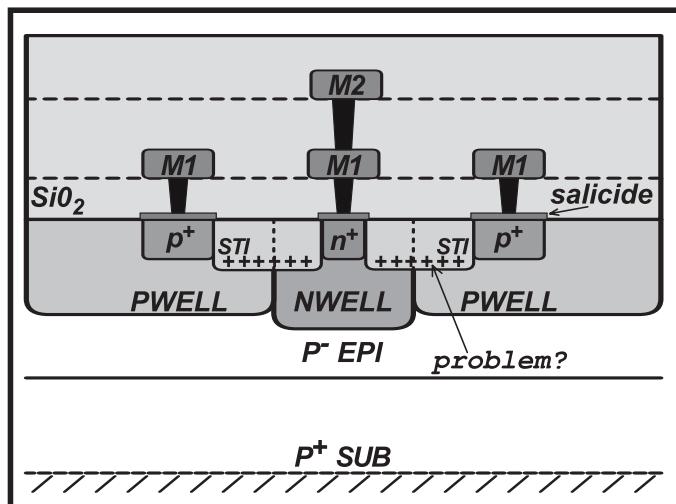


Future prospects - example DDS chip proposal

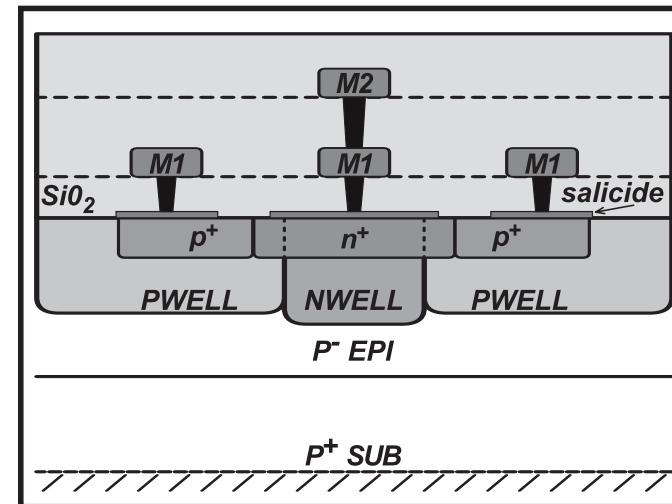


Future prospects

- How to improve radiation hardness?
 - using submicronic processes with enclosed transistors, guard-rings,
 - improving Si-SiO₂ interface conditions in the vicinity of the charge collecting diodes (care to STI, silicides)



Standard structure



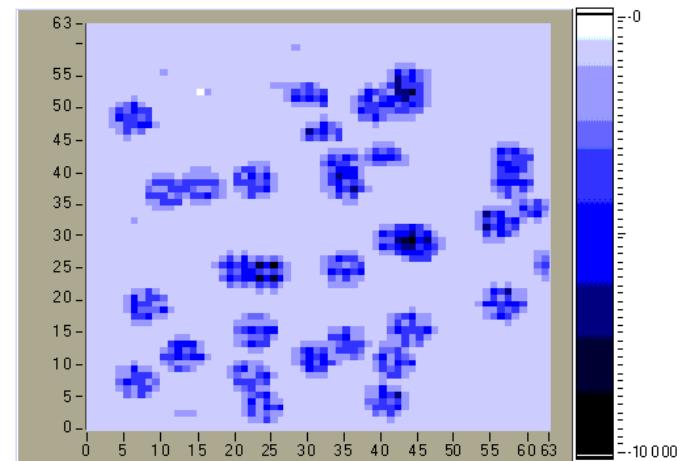
New design (0.25 μm CMOS)



☒ Conclusions

- ☒ Good performance of pixels CMOS demonstrated at small scale of $20 \times 20 \mu\text{m}$ pixels ($\epsilon \sim 99\%$, $S/N \sim 20-40$, $\sigma \sim 1.5-2.5 \mu\text{m}$),
- ☒ The latter needs to be reproduced with large scale chip!
- ☒ Access to processes with epitaxial layer (TSMC 0.25 μm with 8 μm p-type epitaxial layer - optimised for CMOS imagers),
- ☒ Cost effective solution (1900 USD/ 8'' wafer \Rightarrow 9 USD/cm² comparable to simple strip detectors),
- ☒ directions to investigate
 - fabrication of a large size chip - even of very simple architecture,
 - for latter estimation of yield, thinning to 20-50 μm , on-wafer stitching,
 - data processing on-a-chip,
 - radiation hardness
(not so bad... 600 krad and 10^{12} p/cm^2),
 - other sensing elements PG, PPD, PhotoFET.

CMOS APS, apart of photo and video applications, can find their place also in experimental physics for charged particle tracking, also they can be useful in α and β particles imaging, single photon imaging (through HPD), scintillator and phosphor screen readout and high precision neutron imaging,



Katedra Elektroniki
AGH, Krakow

5.486 MeV α particles from a ^{241}Am source with MIMOSA I