Techniques for radiation tolerant design in deep submicron CMOS technologies

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Snowmass, 9th July 2001

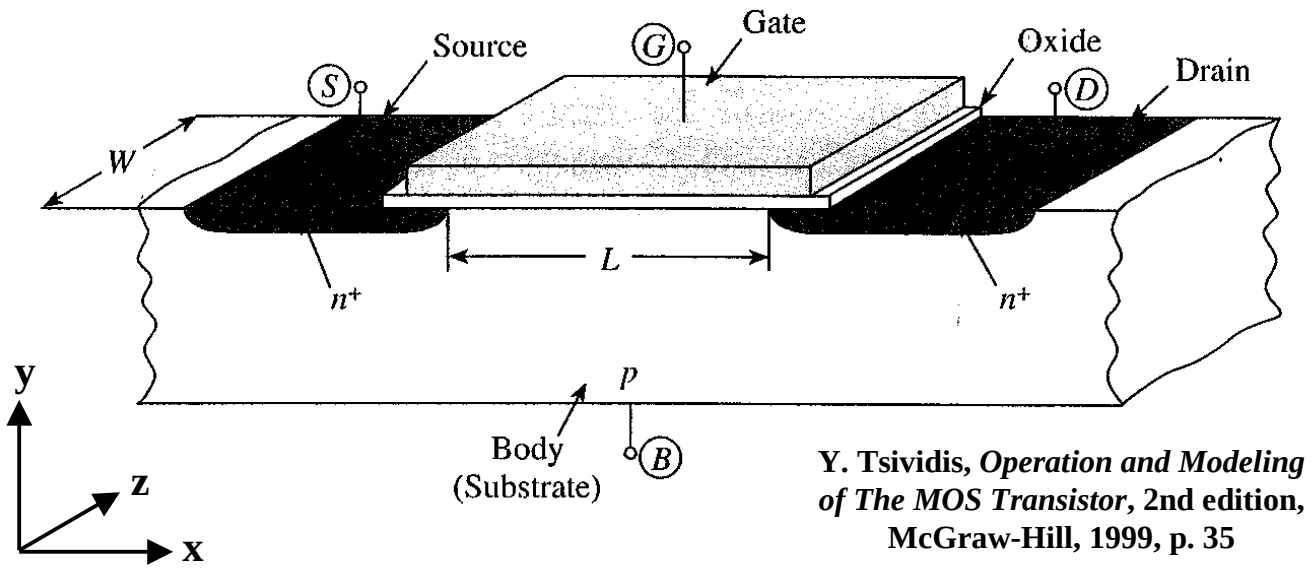
Outline

- CMOS technologies
- The concept of scaling
- Scaling impact on device and circuit performance
- Ionizing radiation effects on CMOS ICs
- Scaling impact on radiation tolerance
- Radiation tolerant design
- Circuit examples
- Conclusions

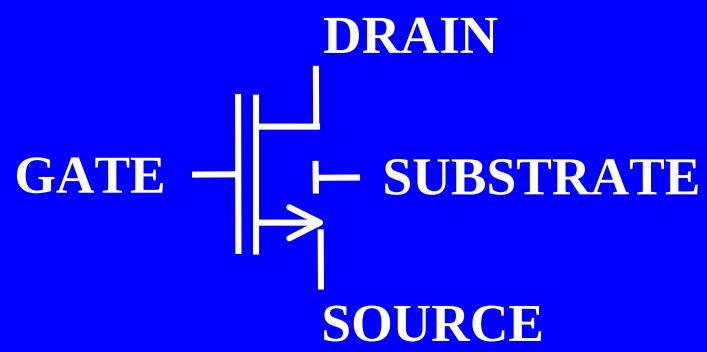
Outline

- CMOS technologies
  - What is a MOS device and how does it work?
  - What is a CMOS technology?
  - Why are CMOS technologies so widespread?
- The concept of scaling
- Scaling impact on device and circuit performance
- Ionizing radiation effects on CMOS ICs
- Scaling impact on radiation tolerance
- Radiation tolerant design
- Circuit examples
- Conclusions

The MOS transistor



Y. Tsividis, *Operation and Modeling of The MOS Transistor*, 2nd edition, McGraw-Hill, 1999, p. 35

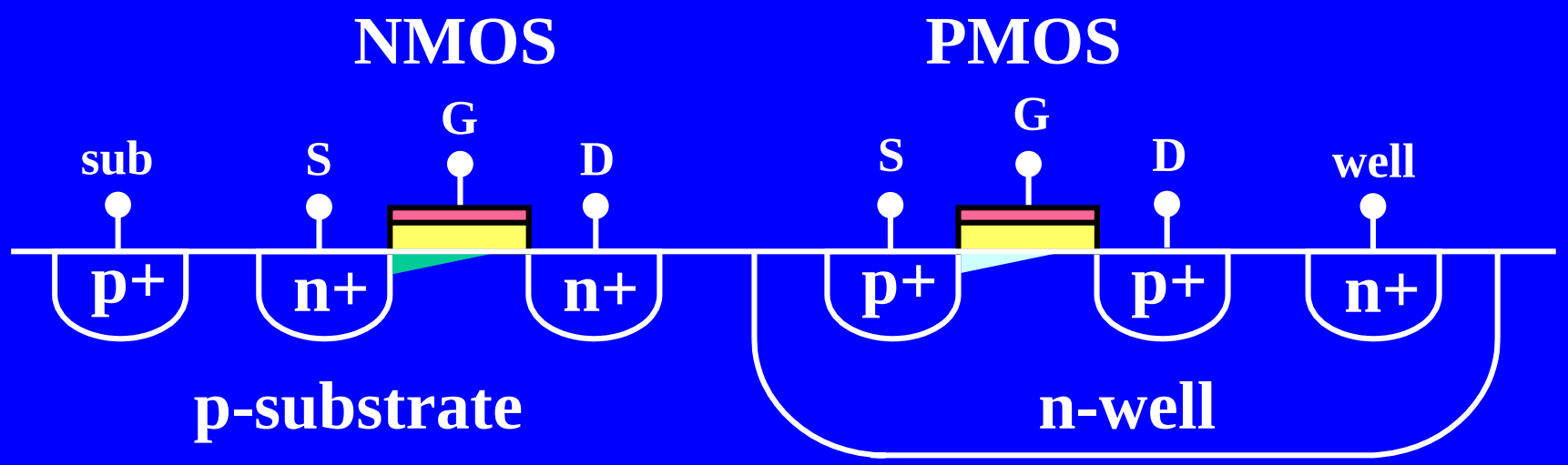


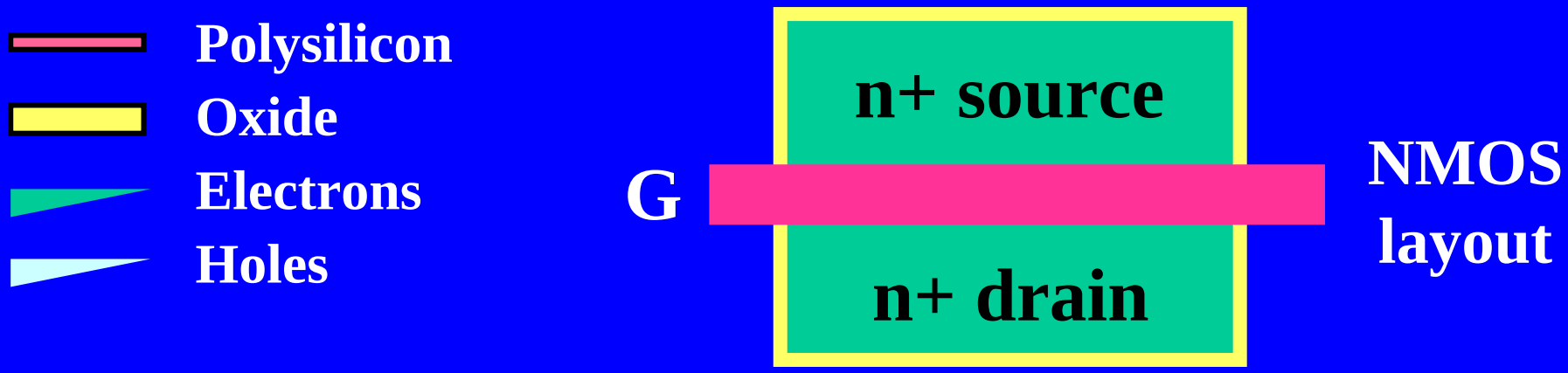
$$i_{DS} = g_m \cdot v_{GS}$$

↓

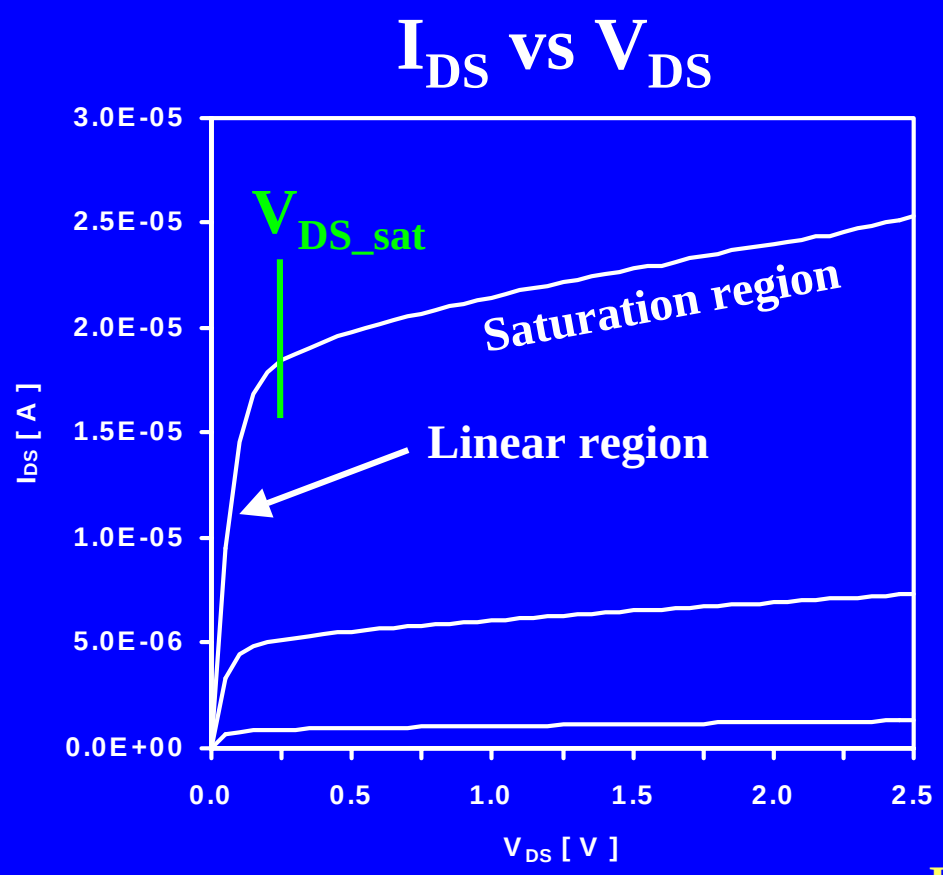
Transconductance

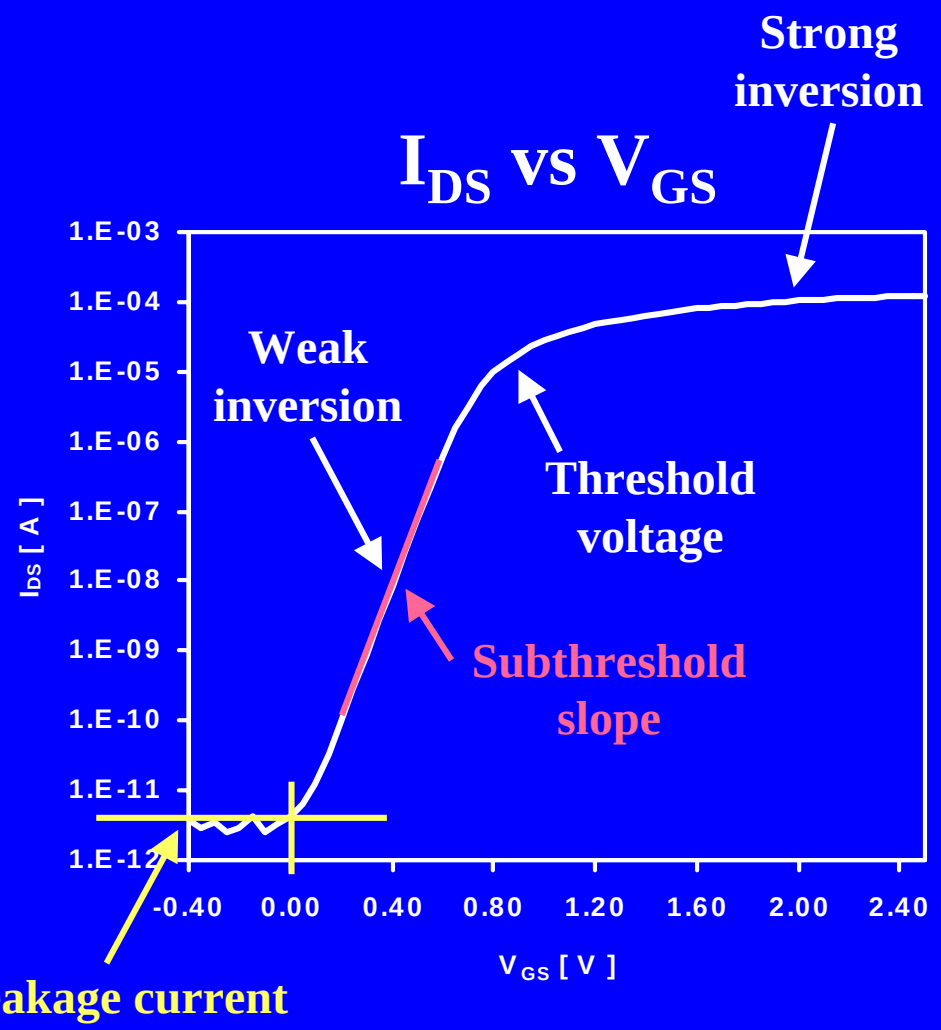
CMOS technology





I - V Characteristics (NMOS)





MOS transistor equations

Strong Inversion

LINEAR REGION

$$I_{DS} = \beta\,(V_{GS} - V_T - \frac{nV_{DS}}{2})V_{DS}$$

SATURATION REGION

$$I_{DS} = \frac{\beta}{2n}(V_{GS} - V_T)^2 \qquad g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \sqrt{2\frac{\beta}{n} I_{DS}}$$

Weak Inversion

$$I_{DS} = I_{D0}\frac{W}{L}e^{\frac{V_{GS}}{n\phi_t}}(1 - e^{-\frac{V_{DS}}{n\phi_t}}) = I_{D0}\frac{W}{L}e^{\frac{V_{GS}}{n\phi_t}} \qquad g_m = \frac{I_{DS}}{n\phi_t}$$

$$V_{DS} > 150\,mV$$

$$\phi_t = \frac{kT}{q} \qquad \beta = \mu\, C_{ox}\frac{W}{L}$$

Why is CMOS so widespread?

- IC market is driven by digital circuits (memories, microprocessors, …)
- Bipolar logic and NMOS - only logic: too high power consumption per gate
- Progress in the manufacturing technology made CMOS technologies a reality
- Modern CMOS technologies offer excellent performance: high speed, low power consumption, VLSI, low cost, high yield

CMOS technologies occupies an increasing portion of the IC market

Outline

- CMOS technologies
- The concept of scaling
  - Moore's law
  - Constant field scaling and generalized scaling
  - Few words about the future of CMOS...
- Scaling impact on device and circuit performance
- Ionizing radiation effects on CMOS ICs
- Scaling impact on radiation tolerance
- Radiation tolerant design
- Circuit examples
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Moore's law

1965: Number of Integrated Circuit components will double every year

G. E. Moore, "Cramming More Components onto Integrated Circuits", *Electronics*, vol. 38, no. 8, 1965.

1975: Number of Integrated Circuit components will double every 18 months

G. E. Moore, "Progress in Digital Integrated Electronics", *Technical Digest of the IEEE IEDM 1975*.

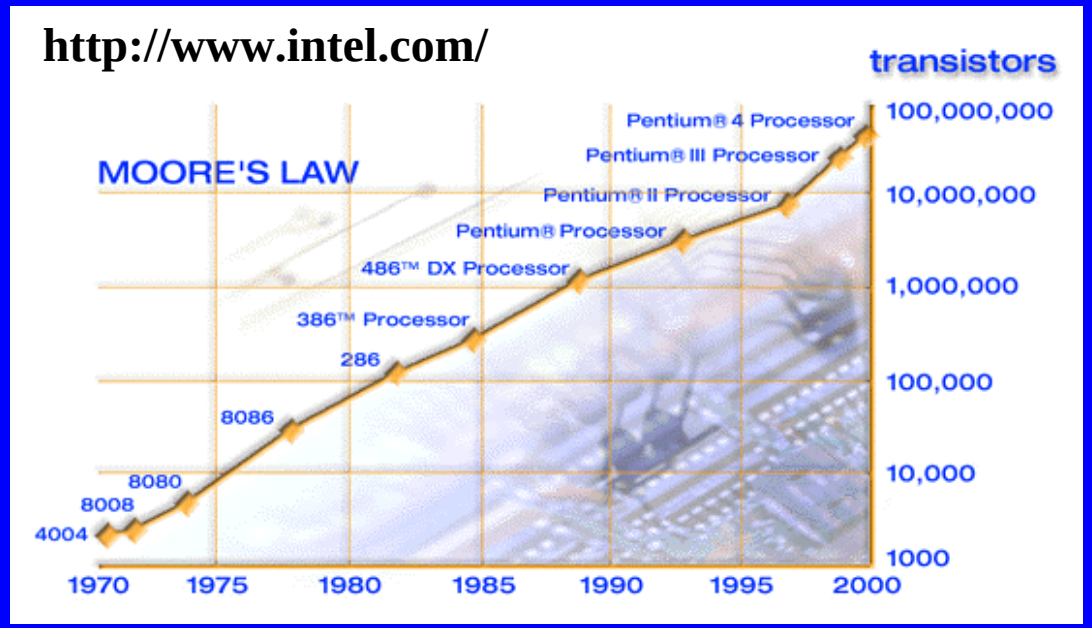
1996: The definition of "Moore's Law" has come to refer to almost anything related to the semiconductor industry that when plotted on semi-log paper approximates a straight line. I don't want to do anything to restrict this definition. - G. E. Moore, 8/7/1996

P. K. Bondyopadhyay, "Moore's Law Governs the Silicon Revolution", *Proc. of the IEEE*, vol. 86, no. 1, Jan. 1998, pp. 78-81.

An example:

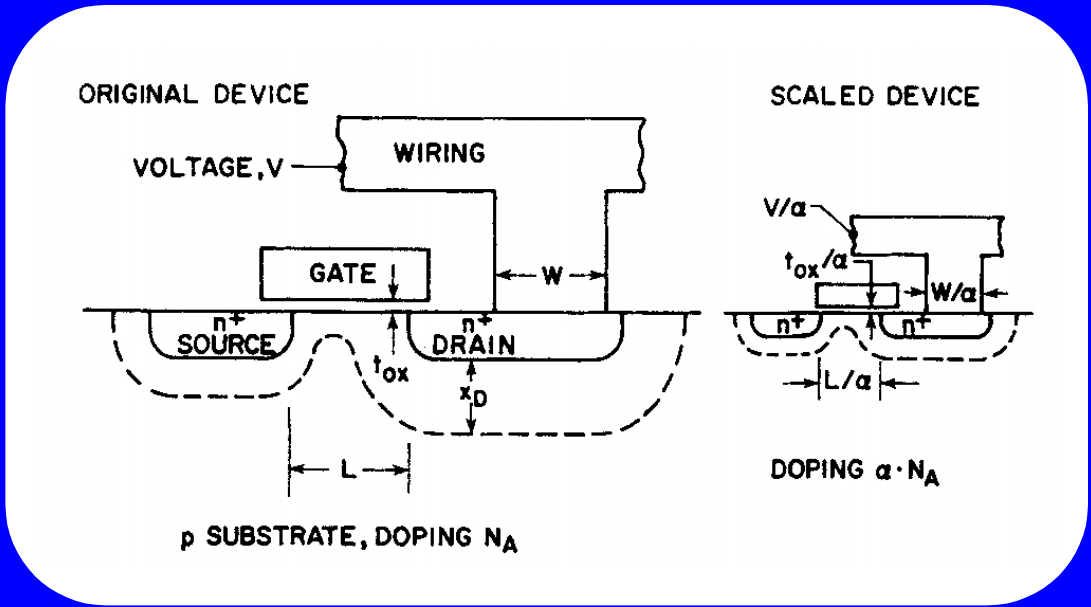
Intel's Microprocessors →

http://www.intel.com/



Constant field scaling

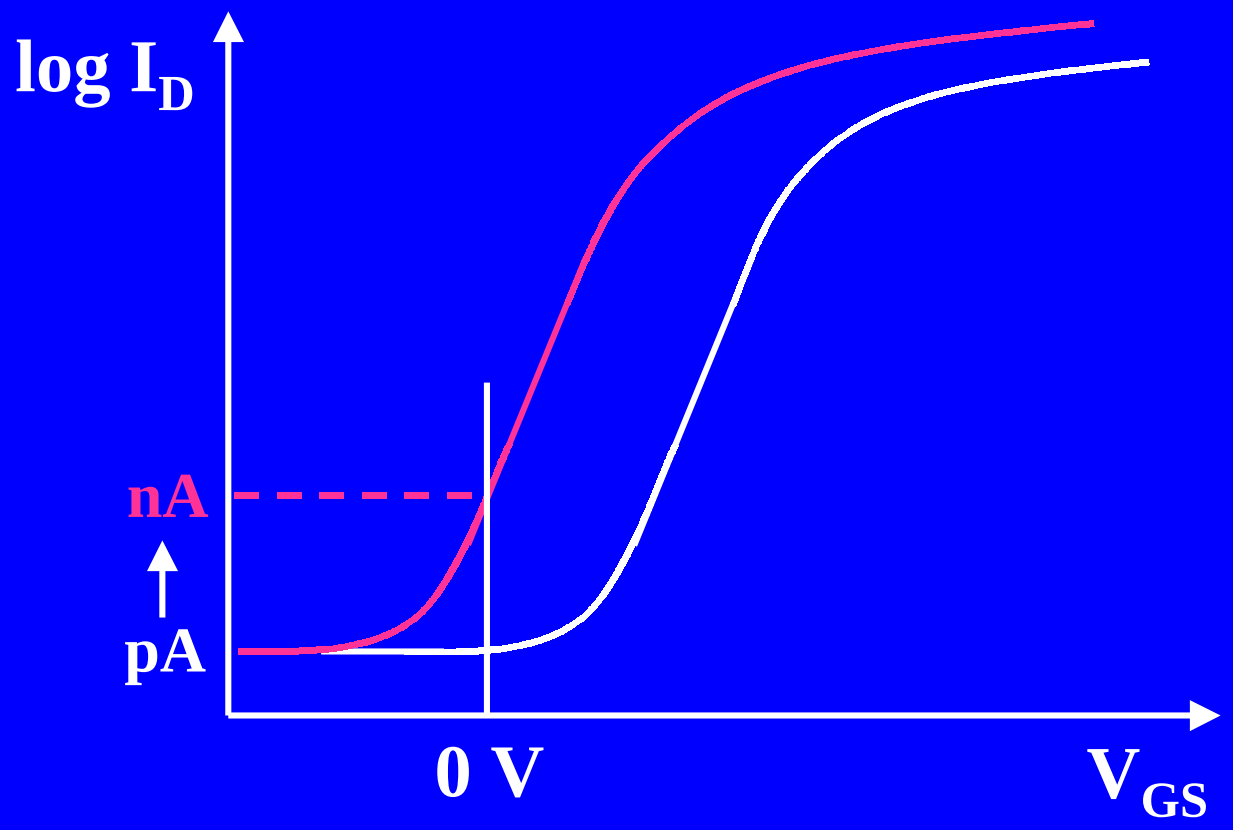
- L, W, t_{ox}, x_D, V, V_T, C, I, τ scale by $1/\alpha$
- Area, Power diss. for a given circuit, Charges scale by $1/\alpha^2$
- Power diss. per unit area, Charges per unit area do not scale



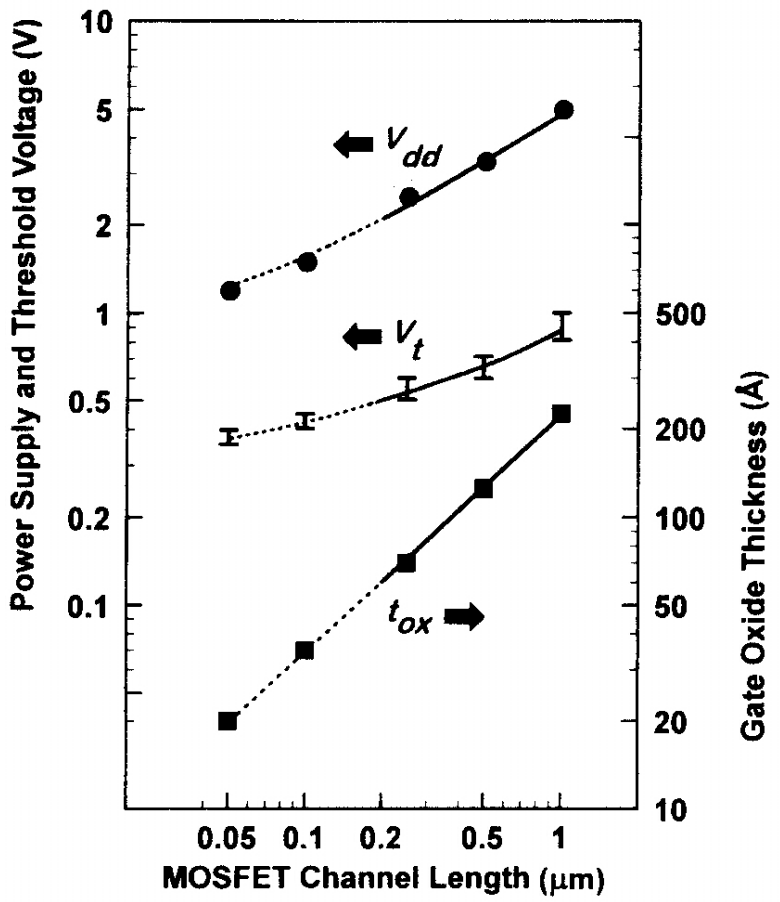
B. Davari et al., "CMOS Scaling for High Performance and Low Power - The Next Ten Years", *Proc. of the IEEE*, vol. 87, no. 4, Apr. 1999, pp. 659-667.

Constant field scaling problem

Subthreshold slope and width of the moderate inversion region do not scale!!!



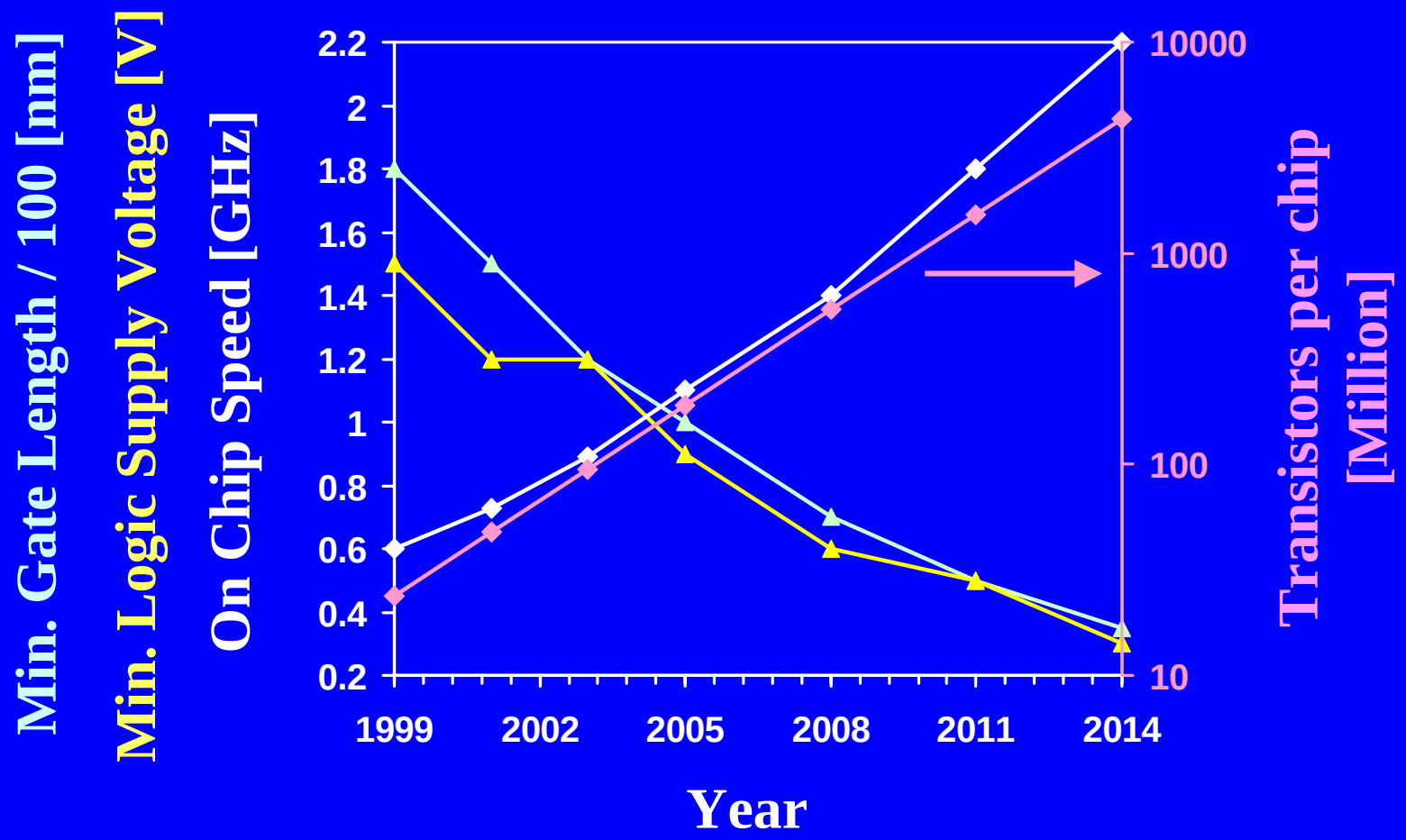
Generalized scaling



- The dimensions in the device scales as in the *constant field* scaling
- V_{dd} scales to have reasonable electric fields in the device, but slower than t_{ox}, to have an useful voltage swing for the signals
- The doping levels are adjusted to have the correct depletion region widths
- To limit the subthreshold currents, V_T scales more slowly than V_{dd}

Y. Taur et al., "CMOS Scaling into the Nanometer Regime", *Proc. of the IEEE*, vol. 85, no. 4, Apr. 1997, pp. 486-504.
Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, 1998, p. 186.

Future perspectives



Semiconductor Industry Association

The International Technology Roadmap for Semiconductors (1999 Edition)

Challenges for the future

- Lithography
- Gate oxide (materials, tunneling, reliability)
- Wiring and interconnections (materials)
- Many metal layers (up to 10)
- Design complexity (CAD tools)
- Low voltage architectures

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- CMOS technologies
- The concept of scaling
- Scaling impact on device and circuit performance
  - Digital circuits
  - Analog circuits (noise, matching, power consumption)
- Ionizing radiation effects on CMOS ICs
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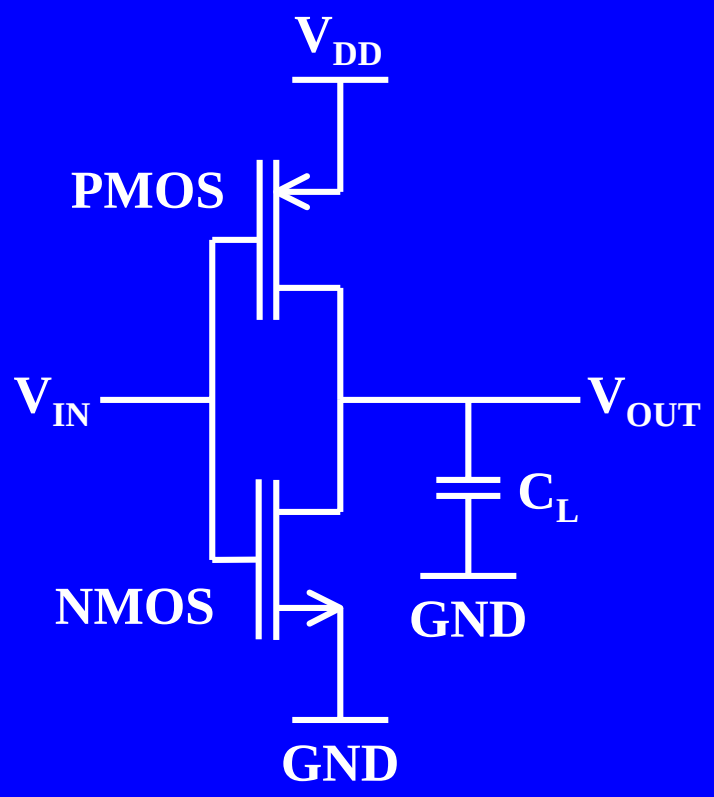
Scaling impact on digital circuits

Example: CMOS inverter



$$P_{static} = I_{leakage} \cdot V_{DD}$$

$$P_{dynamic} = C_L \cdot V_{DD}^2 \cdot f$$

$$PDP = C_L \cdot V_{DD}^2$$

Power-delay product

t_{ox} ↓ V_{DD} ↓ C_L ↓

Scaling improves density, speed and power consumption!

MOST noise power spectral density

$$\frac{\overline{v_{in}^2}}{\Delta f} = 4kTn\gamma \frac{1}{g_m} + \frac{K_a}{C_{ox}^2\, WL} \frac{1}{f^{\alpha}}$$

Channel thermal noise

1/f noise

$$\gamma = F(I) \cdot \Gamma$$

F(I) varies from 1/2 (w.i.) to 2/3 (s.i.)

Γ = Excess noise factor

K_a = 1/f noise parameter

Scaling impact on noise

For the same device dimensions and current, both the channel thermal noise and the flicker (1/f) noise should decrease

BUT

there can be other effects in submicron MOSFETs that tend to increase the noise, as for example:

carriers heating, gate tunneling current, parasitic resistances, ...

Matching of IC components

Matching is the statistical study of the differences between the electrical parameters of identically designed components placed at a small distance in an identical environment and used with the same bias conditions.

To characterize the mismatch between transistors we:

- **Design transistor pairs of different dimensions**
- **Measure V_T and β for each transistor of each pair**
- **Calculate ΔV_T and $\Delta \beta/\beta$ for each pair**
- **Extract $\sigma_{\Delta Vth}$ and $\sigma_{\Delta \beta/\beta}$ from the two distributions**

Expected mismatch

$$\sigma_{\Delta V_{th}} = \frac{A_{V_{th}}}{\sqrt{W\,L}} \qquad A_{V_{th}} = \sqrt{A_N^2 + A_{IT}^2 + \ldots}$$

$$A_N = \mathrm{Const} \cdot \frac{t_{ox}}{\varepsilon_{ox}} \cdot \sqrt[4]{N}$$

$$A_{IT} = \sqrt{2} \cdot \frac{q \cdot t_{ox}}{\varepsilon_{ox}} \cdot \sqrt{N_{IT}}$$

$$\sigma_{\Delta\beta/\beta} = \frac{A_\beta}{\sqrt{W\,L}}$$

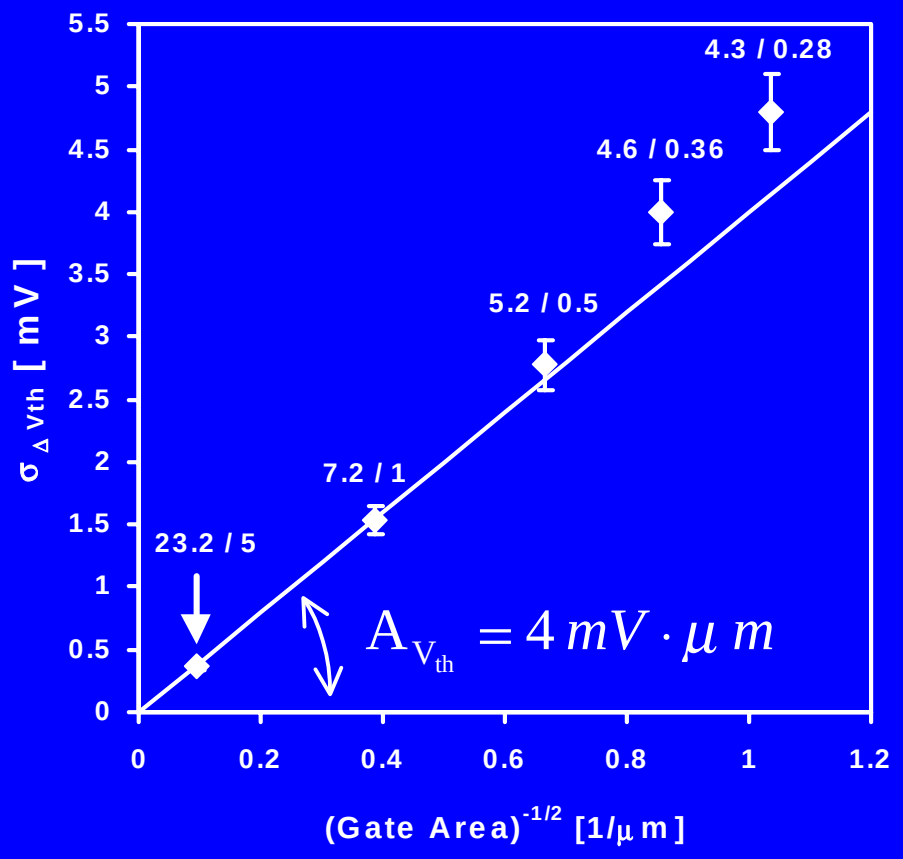
A_N (channel dopant fluctuation) / t_{ox} ~ 0.5 mV·µm / nm

A_{Vth} / t_{ox} ~ 1 mV·µm / nm

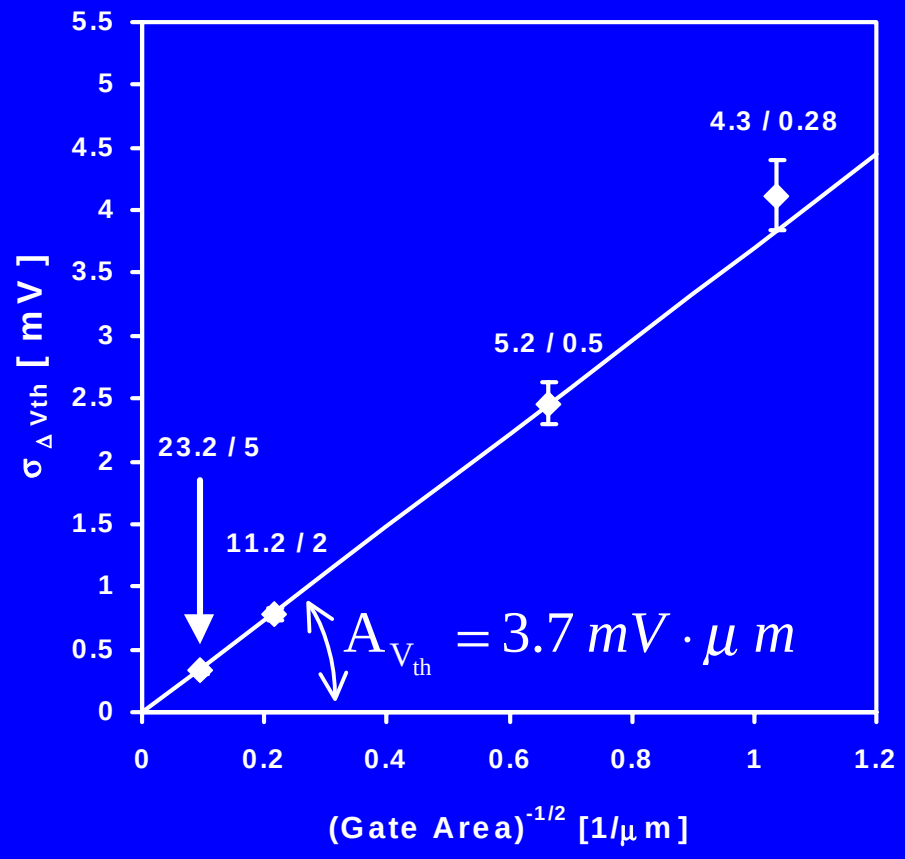
A_β ~ 1 to 3 %·µm

MOST V_T mismatch

N-channel



P-channel



0.25 μm technology - t_{ox} = 5 nm

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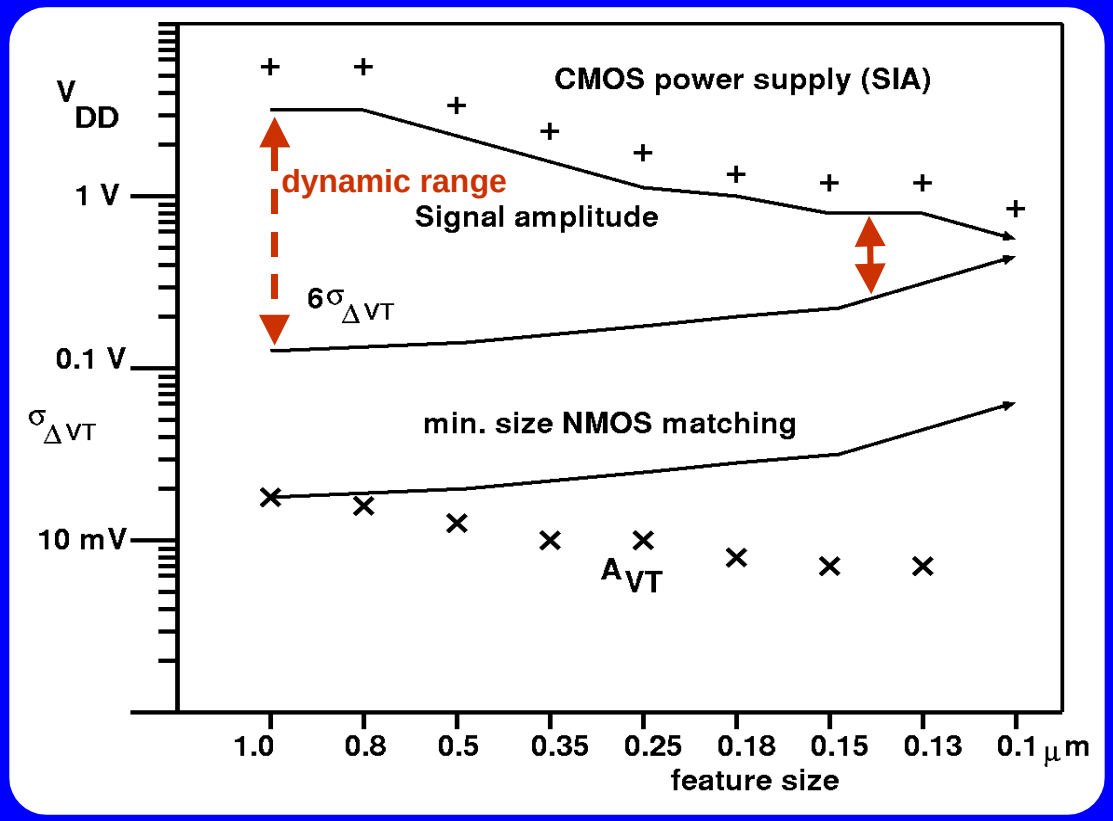
Scaling impact on V_T matching



M.J.M. Pelgrom et al., "Transistor matching in analog CMOS applications", *Technical Digest of the International Devices Meeting 1998*, pp. 915-918.

Matching will limit the potential performance in sub-micron

Analog power consumption

t_{ox} scales ⟶ V_{DD} must be scaled as well

Min. power consumption for class A analog circuits:

$$P_{\min} = 8\pi kT \cdot SNR \cdot f_{sig} \cdot \frac{V_{DD}}{V_{DD} - \Delta V}$$

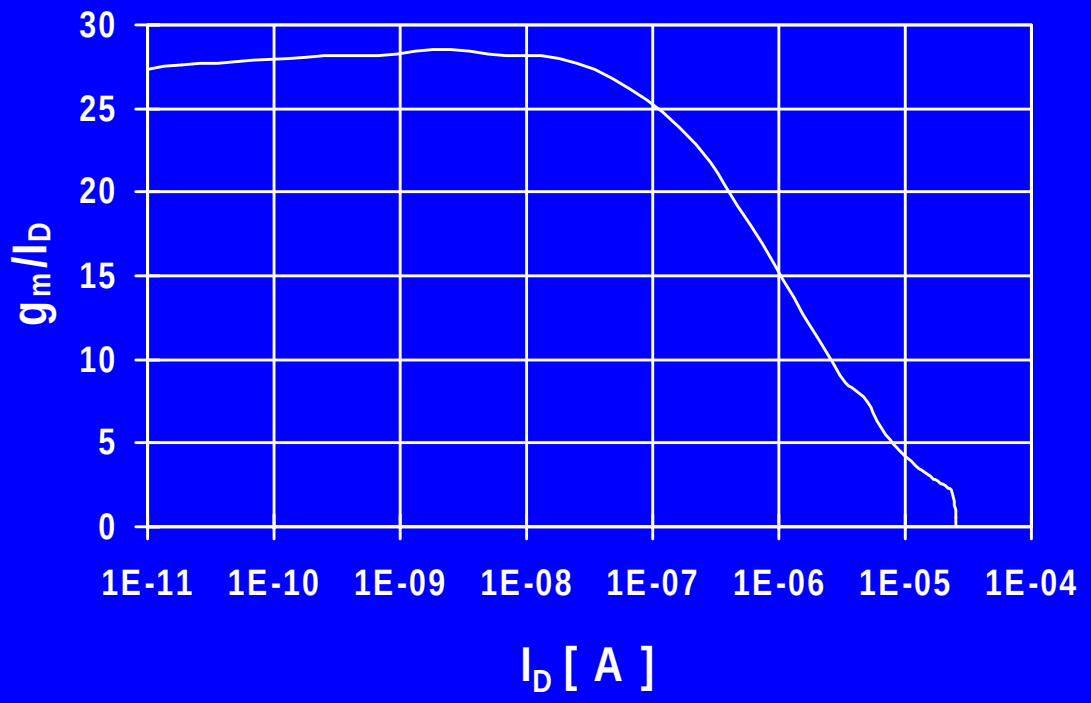
ΔV is the fraction of the V_{DD} not used for signal swing

Optimal analog power/performance trade-off for 0.35 - 0.25 μm technologies

A.-J. Annema, "Analog Circuit Performance and Process Scaling", *IEEE Transactions on Circuit and System II*, vol. 46, no. 6, June 1999, pp. 711-725.

Weak inversion region

t_{ox} scales ⟶ for the same device dimensions the boundary between weak inversion and strong inversion moves towards higher currents



Strong inversion

$$g_m = \sqrt{2\frac{\beta}{n} I_{DS}}$$

Weak inversion

$$g_m = \frac{I_{DS}}{n\phi_t}$$

$$I_{DS_W_to_S} = 2\beta\, n\phi_t^2$$

Scaling impact on analog circuits

t_{ox} scales $\longrightarrow$ for the same device dimensions

- Threshold voltage matching improves $\sigma_{\Delta V_{th}} = \dfrac{\mathrm{Const} \cdot t_{ox}}{\sqrt{W\,L}}$

- 1/f noise decreases $\dfrac{\overline{v_{in}^2}}{\Delta f} = \dfrac{K_a}{C_{ox}^2\,WL}\dfrac{1}{f^{\alpha}}$

- Transconductance increases (same current) $g_m = \sqrt{\dfrac{2}{n}\mu\, C_{ox}\dfrac{W}{L} I_{DS}}$

Scaling impact on analog circuits

- New noise mechanisms
- Modeling difficulties
- Lack of devices for analog design
- Reduced signal swing (new architectures needed)
- Substrate noise in mixed-signal circuits
- Velocity saturation. Critical field: 3 V/μm for electrons,

  10 V/μm for holes

$$g_{m_vel.sat.} = WC_{ox}v_{sat}$$

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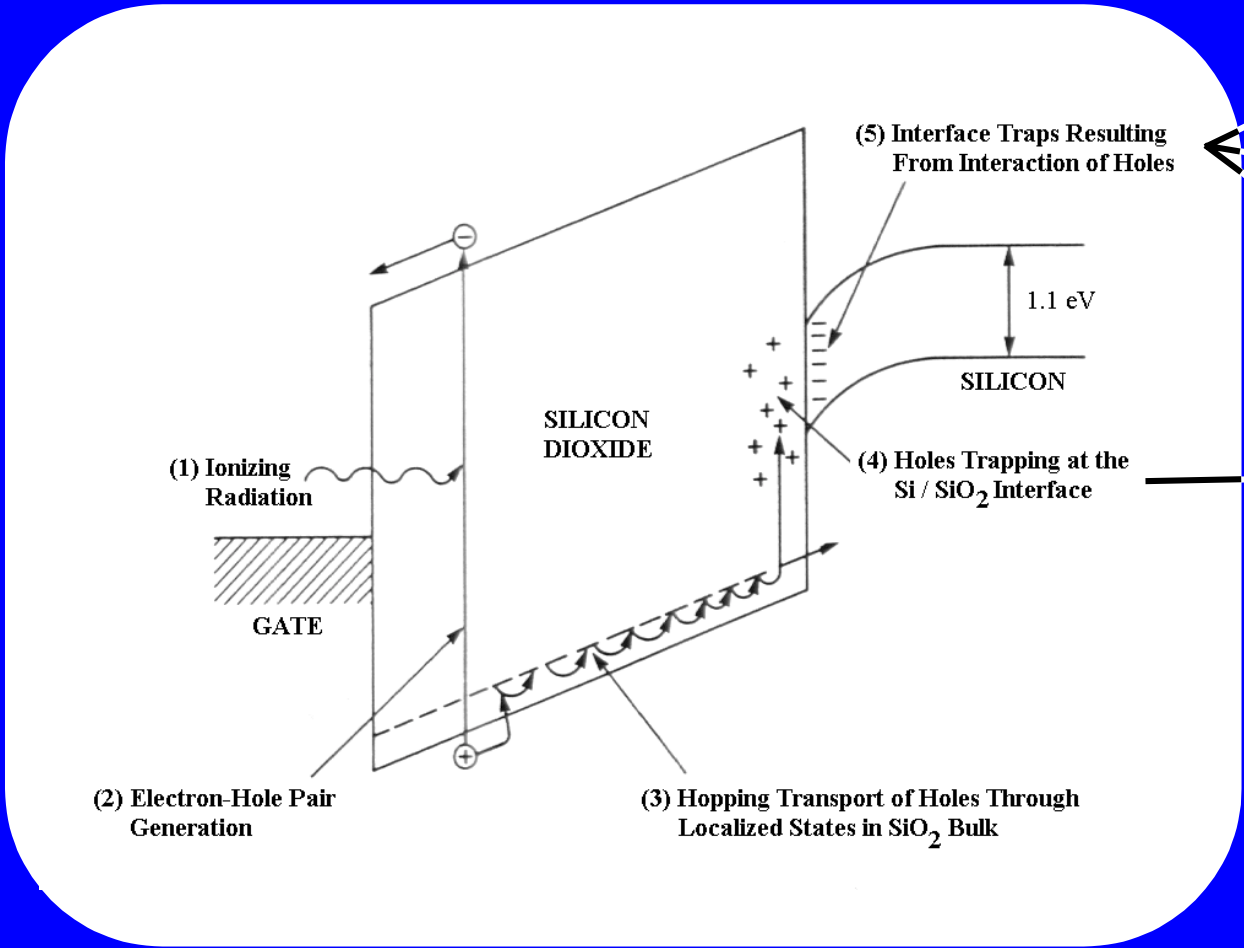
Ionizing particles through a MOST



Threshold voltage shift

Mobility degradation

Subthreshold slope degradation

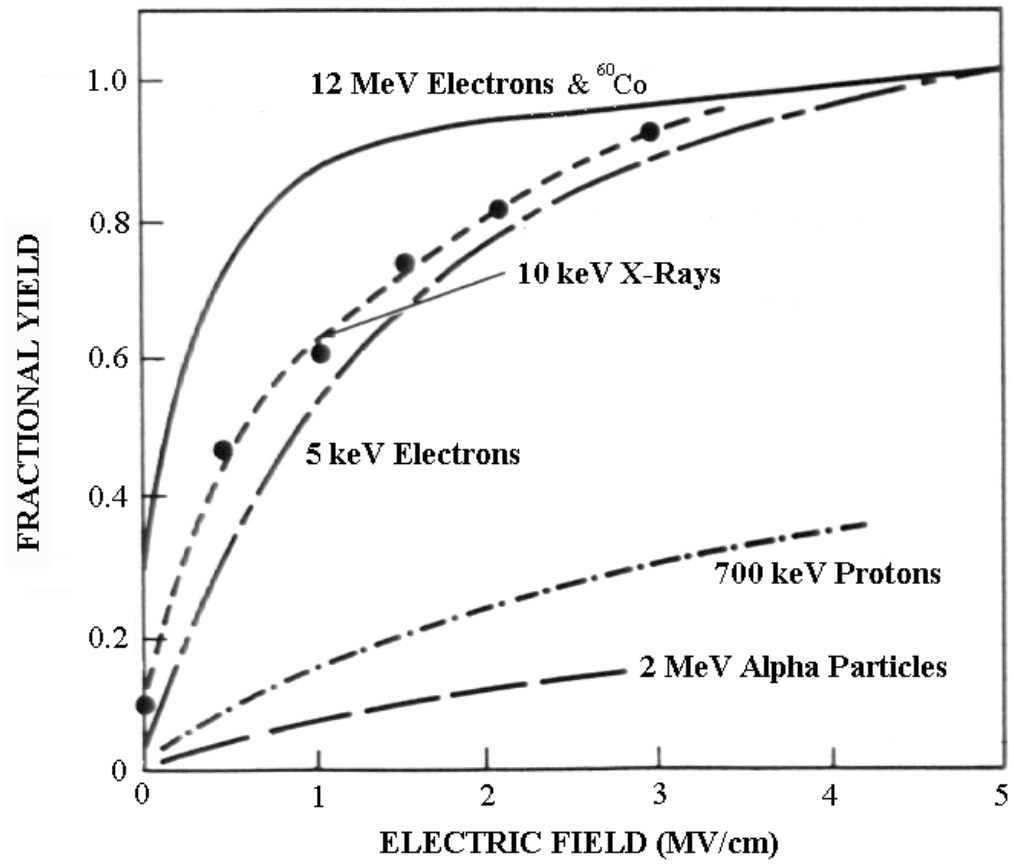
Threshold voltage shift

Other degradations:

- **Transconductance**
- **Noise**
- **Matching**

F. B. McLean and T. R. Oldham, Harry Diamond Laboratories Technical Report, No. HDL-TR-2129, September 1987.

Electron-hole pairs recombination

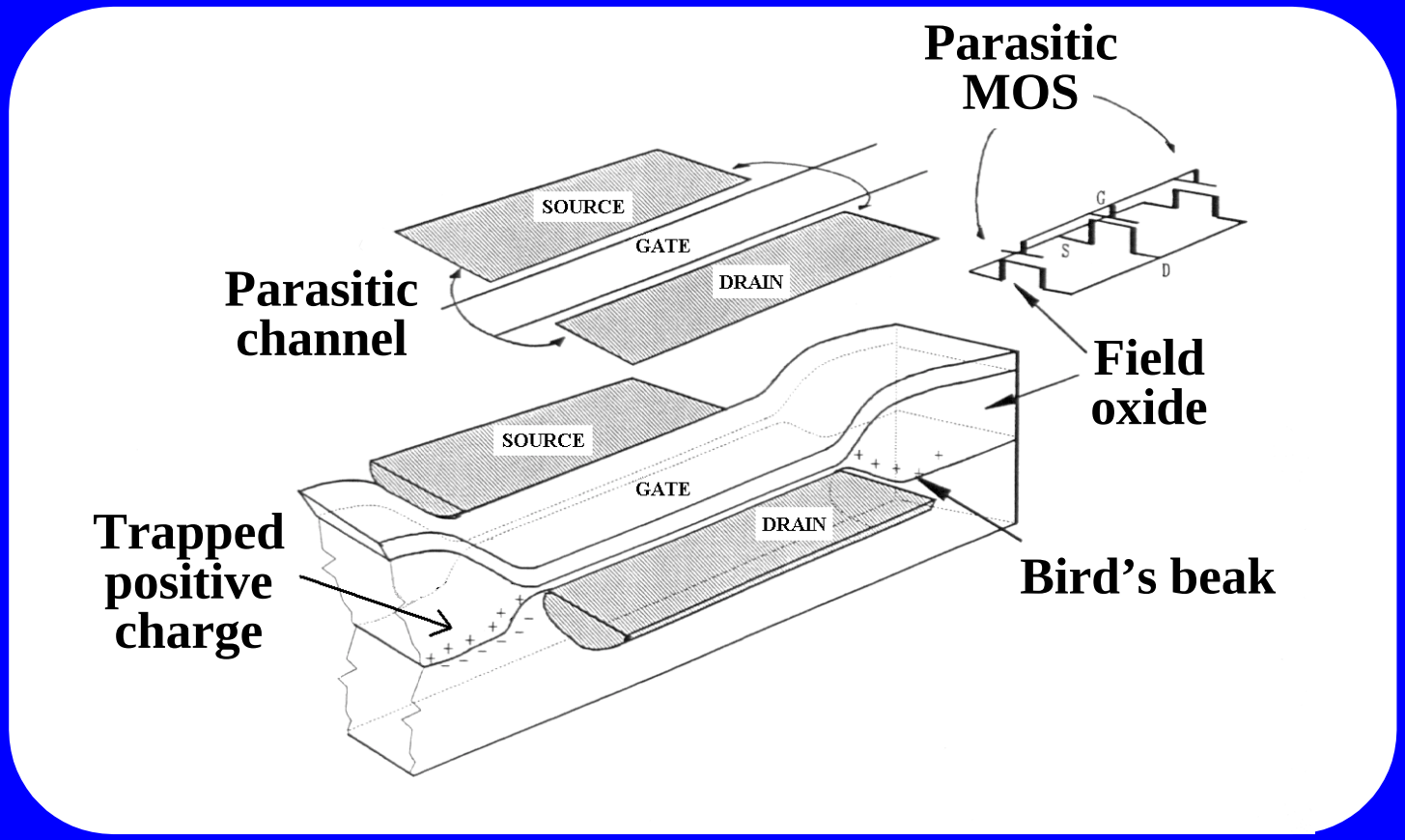


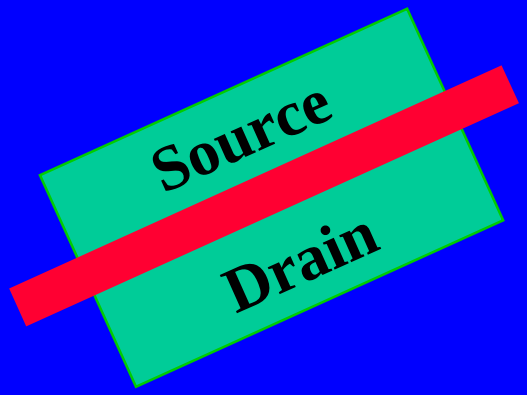
Contributions to the V_T shift

	Oxide charges	Interface states	Total
NMOS	—	+	+ or —
PMOS	—	—	—

- For deep submicron processes the sign of the V_T shift for NMOS transistors tends to be positive
- The bias conditions during irradiation have a great influence on the absolute value of the V_T shift

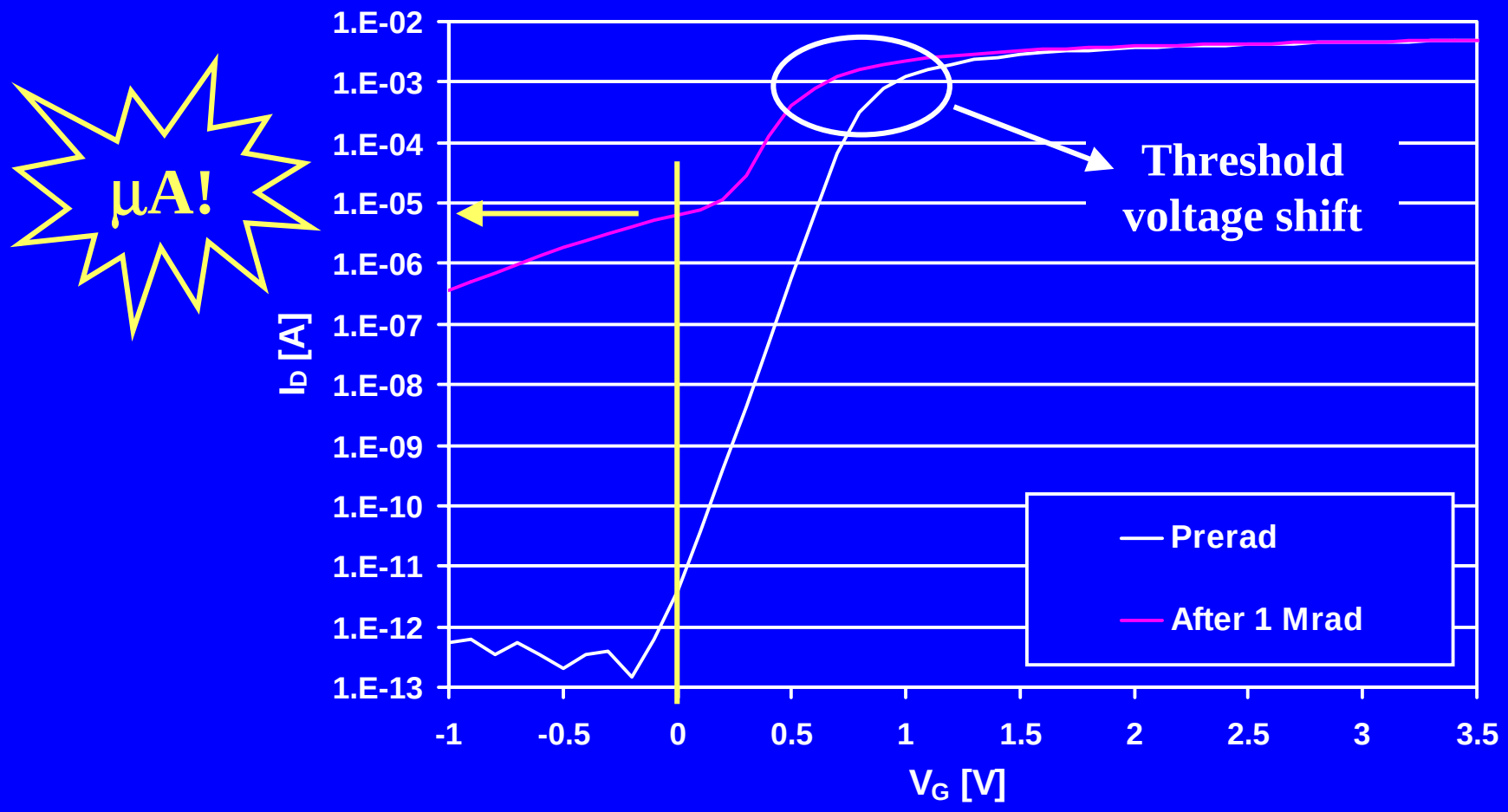
Transistor level leakage (NMOS)





R. Gaillard, J.-L. Leray, O. Musseau et al., "Techniques de durcissement des composant, circuits, et systemes electroniques", Notes of the Short Course of the 3rd European Conference on Radiation and its Effects on Components and Systems, Arcachon (France), Sept. 1995.

Transistor level leakage (NMOS)



0.7 µm technology - t_{ox} = 17 nm

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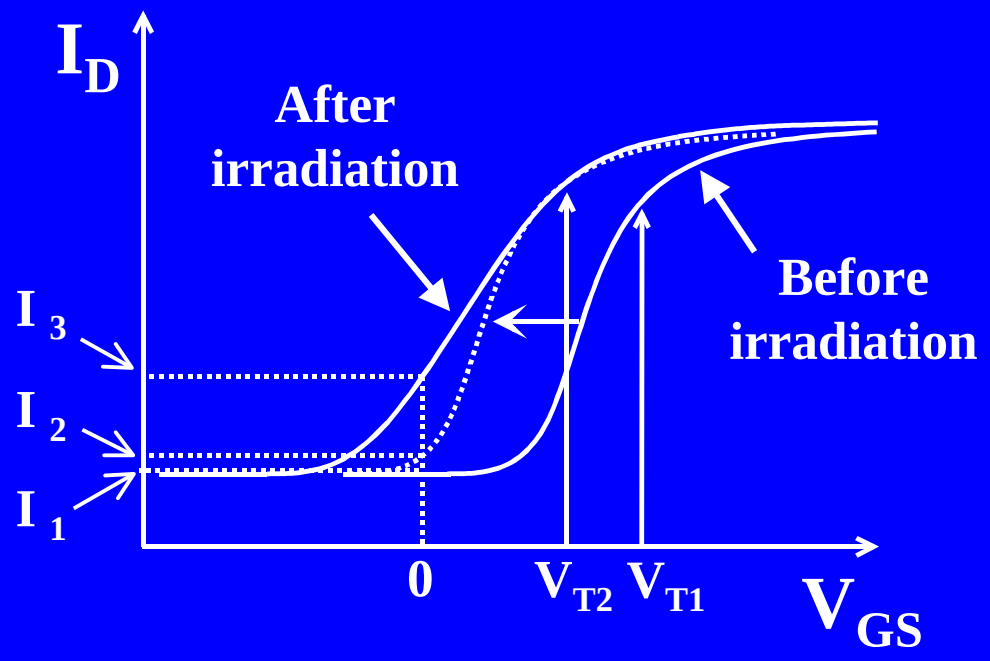
Off-state current increase (?)

Only for n-channel transistors

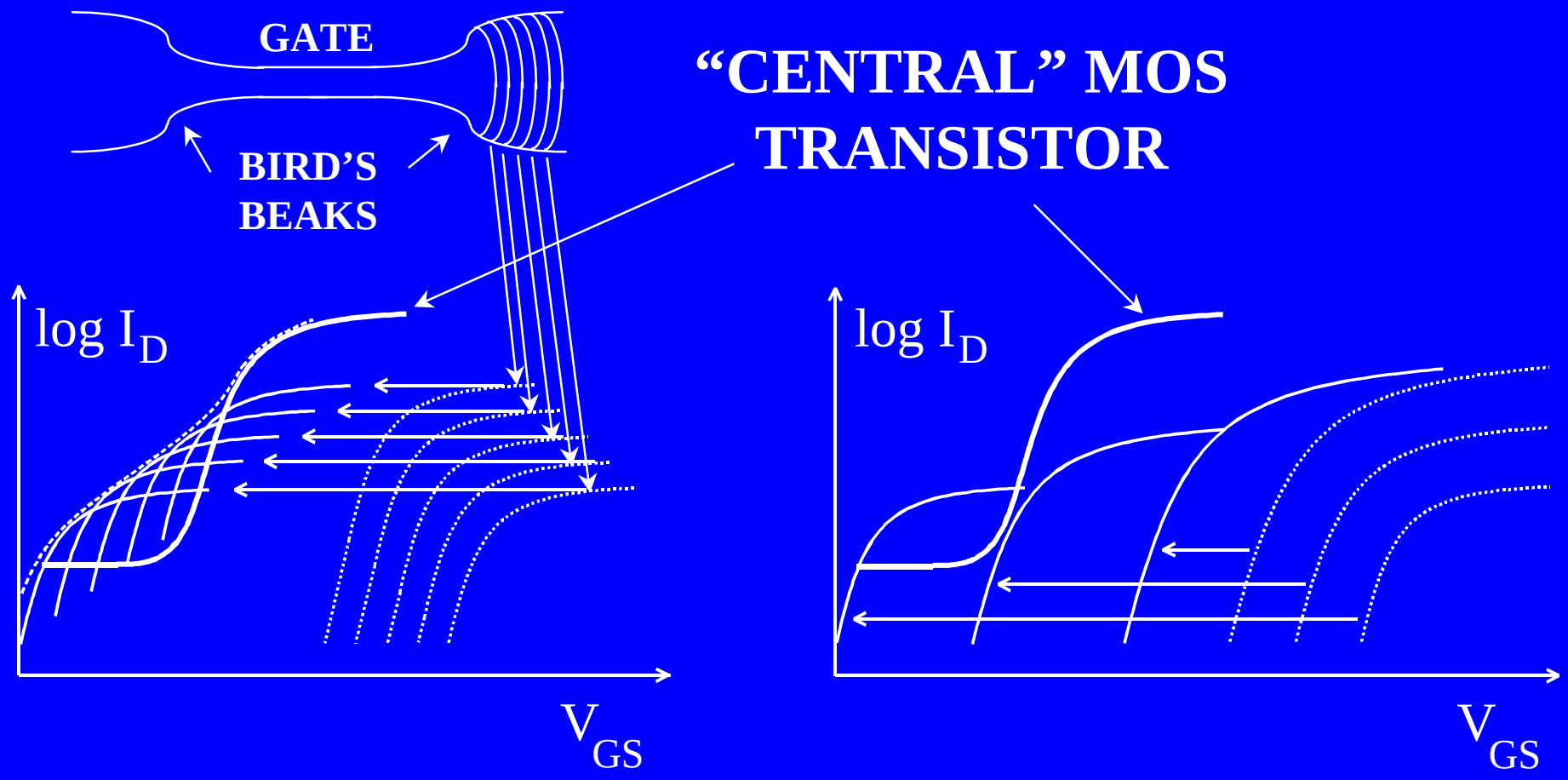
Negative threshold voltage shift

+

Increase in the subthreshold slope

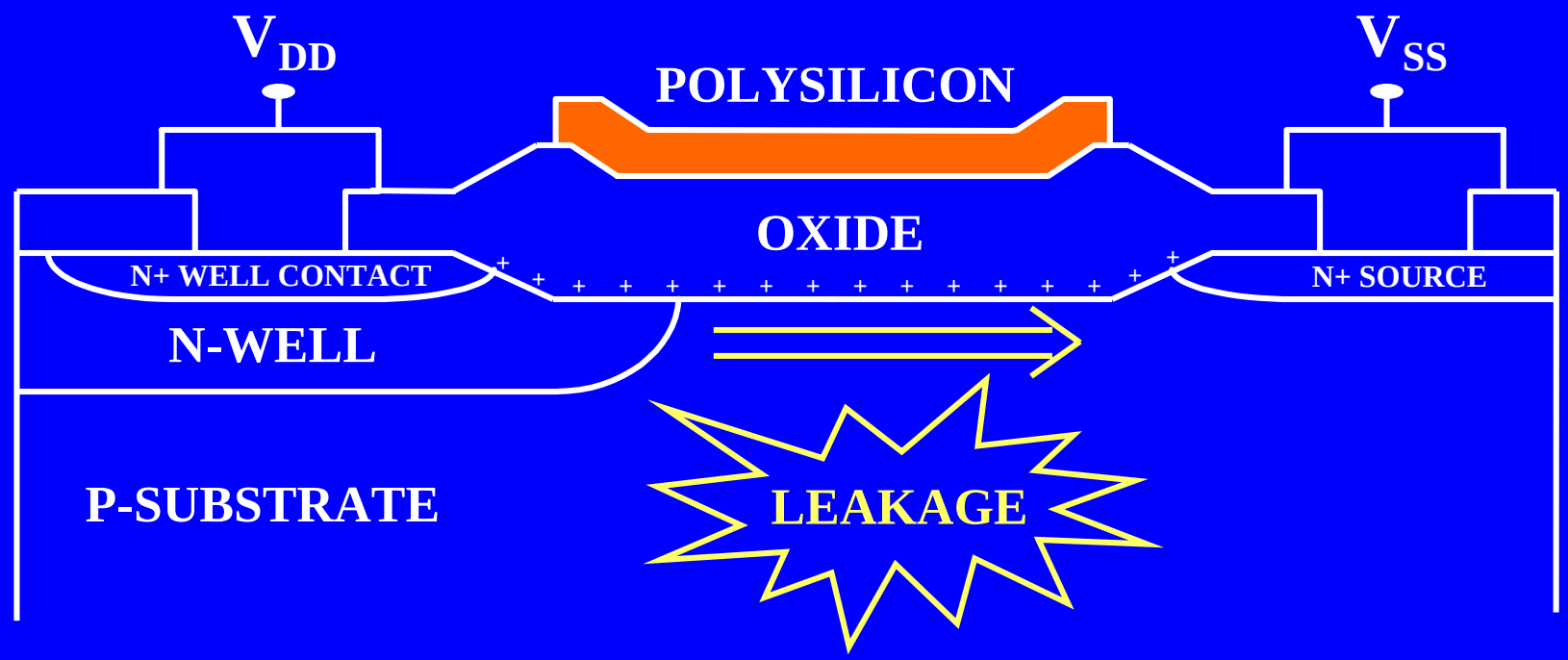


Parasitic currents increase

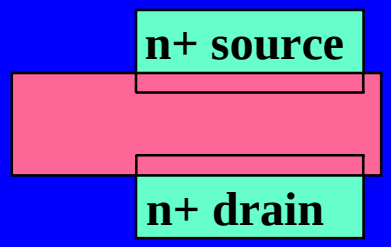


The quality of the field oxide is very important

Integrated circuit level leakage



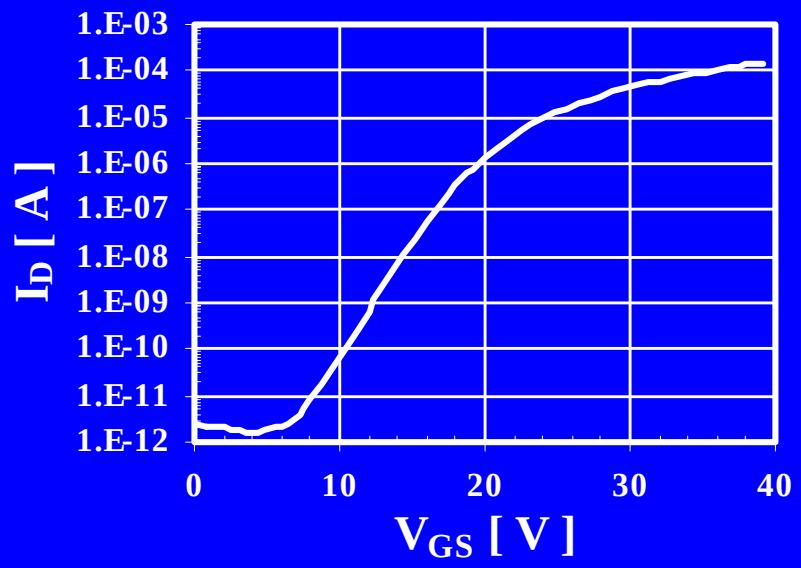
The Field Oxide Transistor



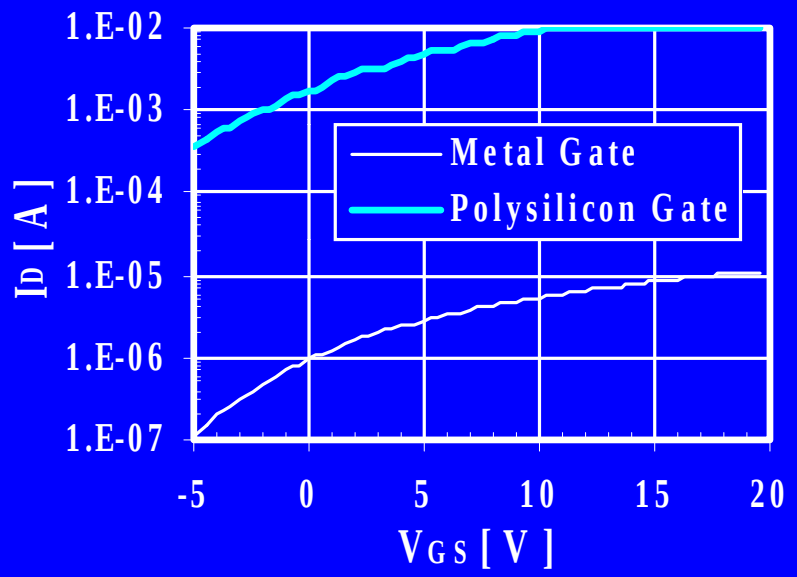
Post-irradiation leakage currents depend on

- Total Dose
- Bias conditions
- Gate Material
- Field oxide quality

PRERAD



AFTER 1 Mrad



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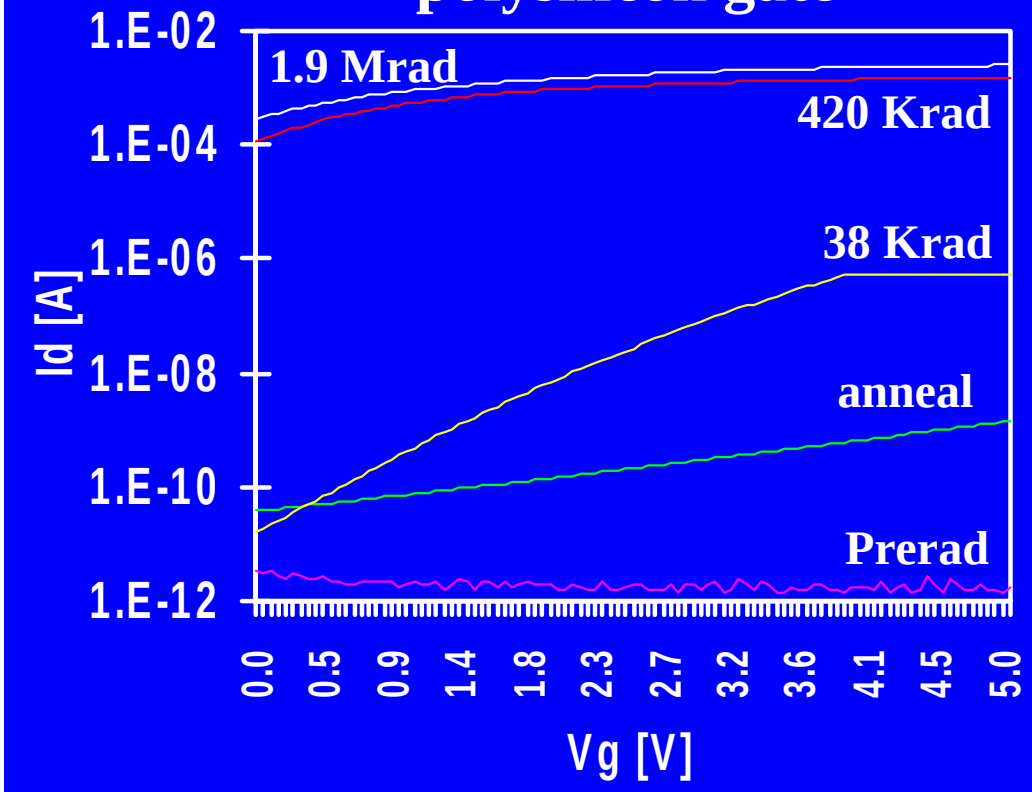
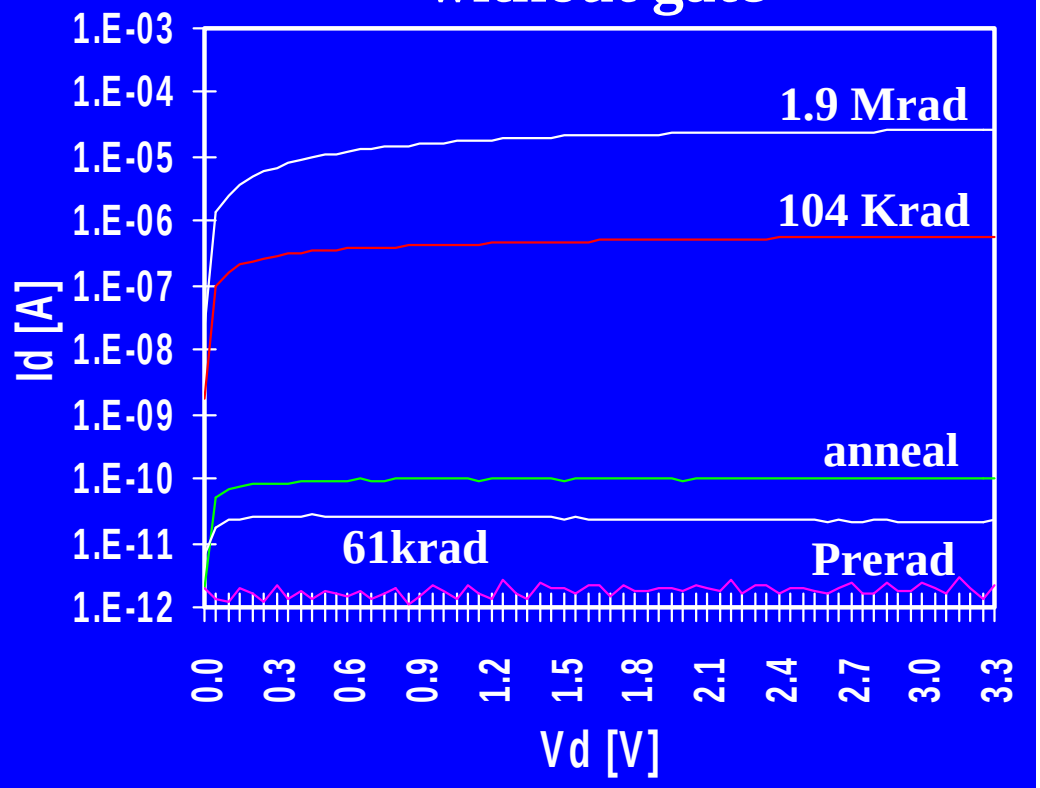
Integrated circuit level leakage

Field oxide leakage - 0.5 μm technology

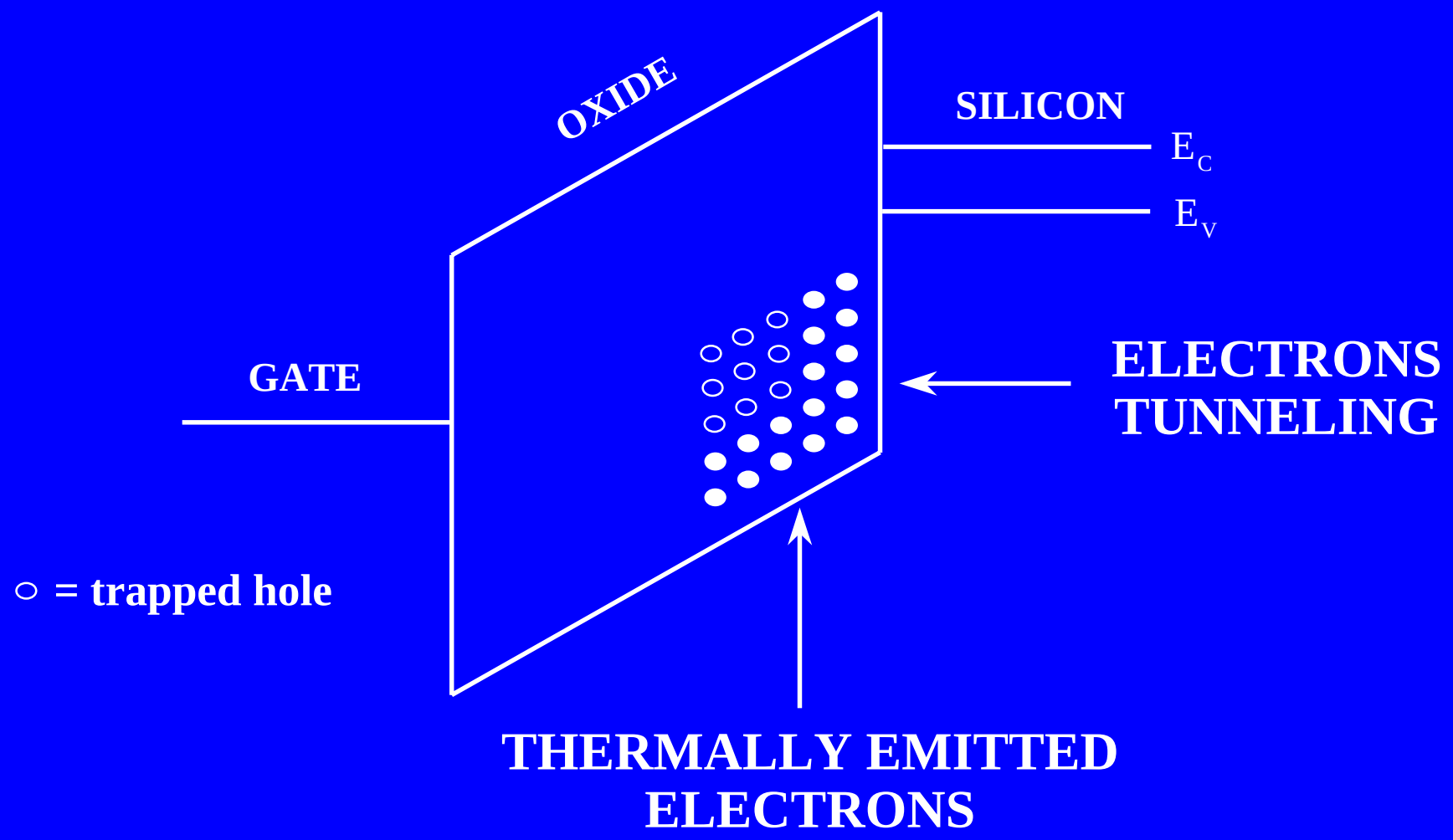
FOXFET 10/1 with polysilicon gate



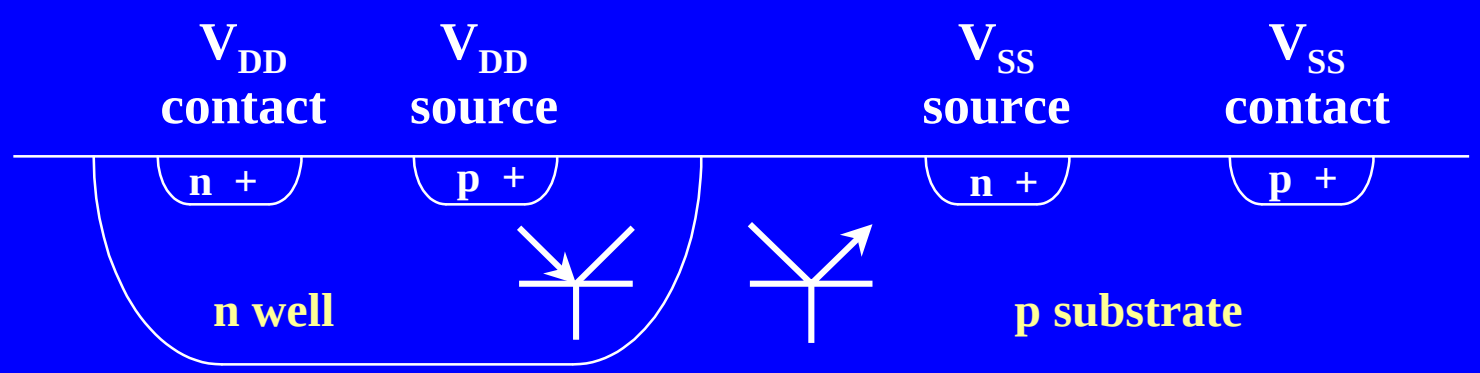
FOXFET 10/1.4 without gate

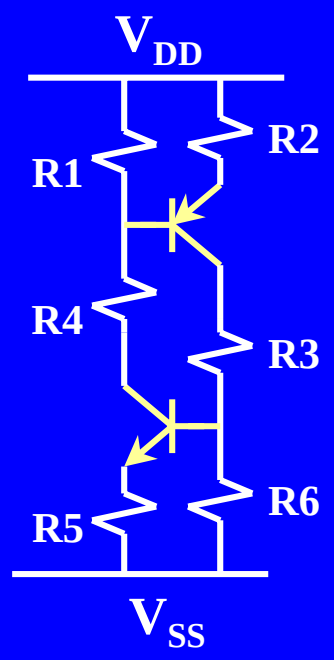


Annealing (mainly in the oxide!)



Single Event Latch-up (SEL)



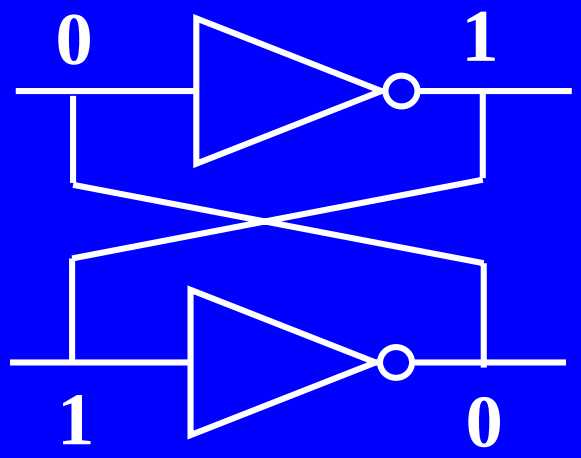


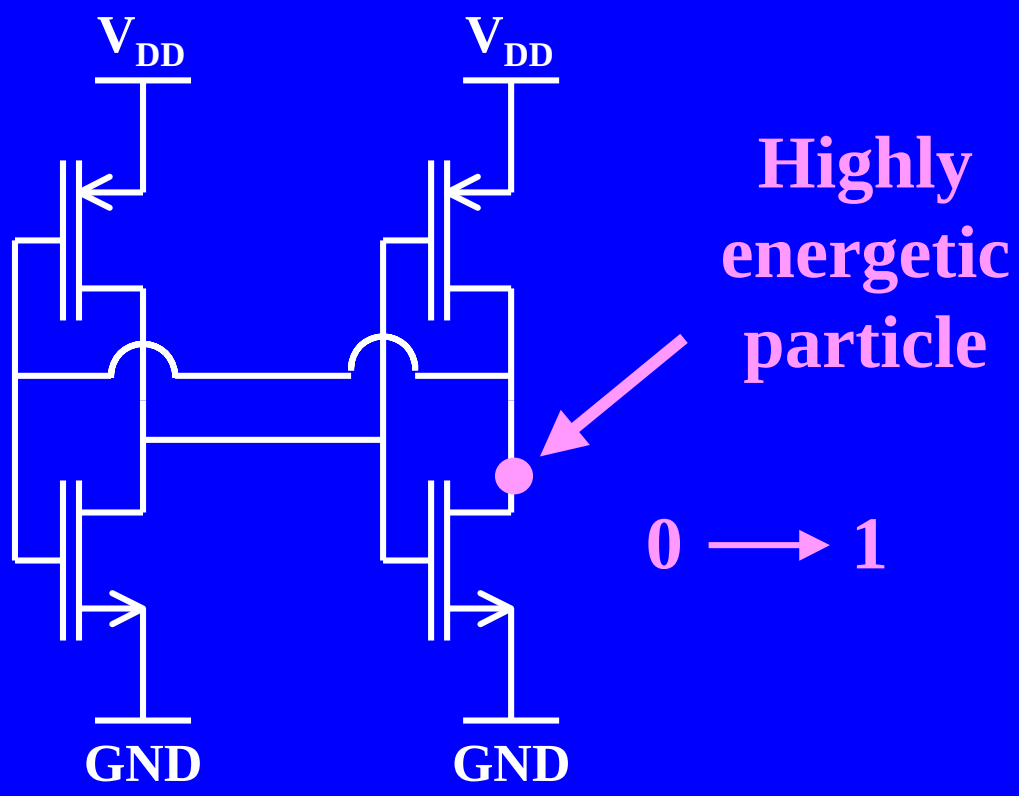
Electrical latch-up might be initiated by electrical transients on input/output lines, elevated temperatures or improper sequencing of power supply biases. These modes are normally addressed by the manufacturer.

Latch-up can be initiated by ionizing particles (SEL)

Single Event Upset (SEU)

Static RAM cell





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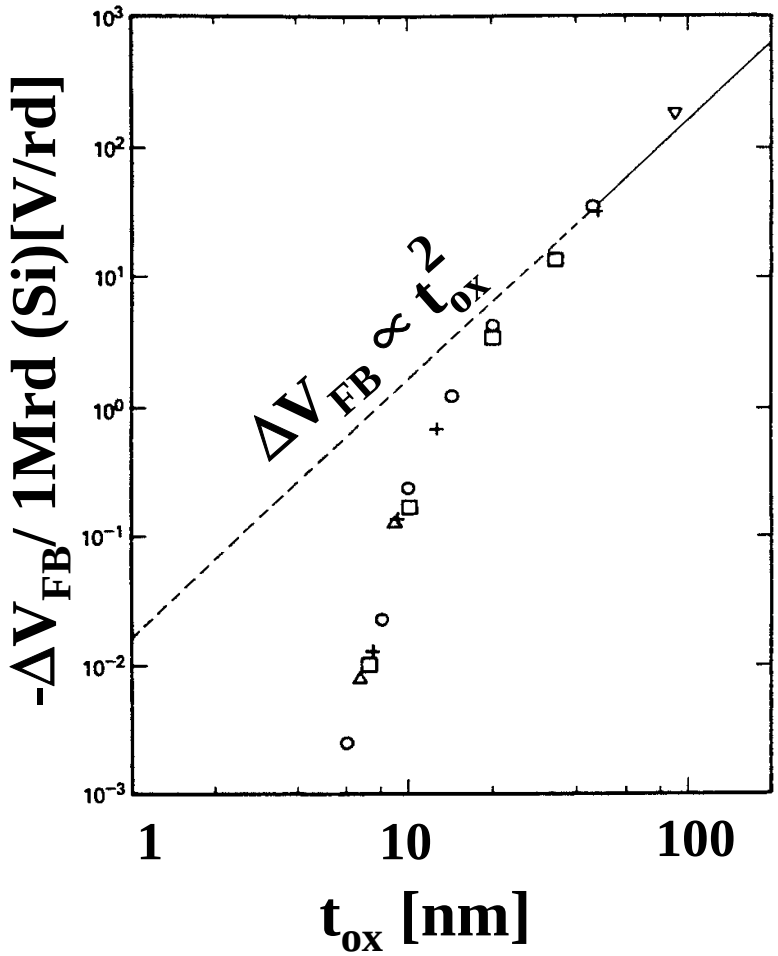
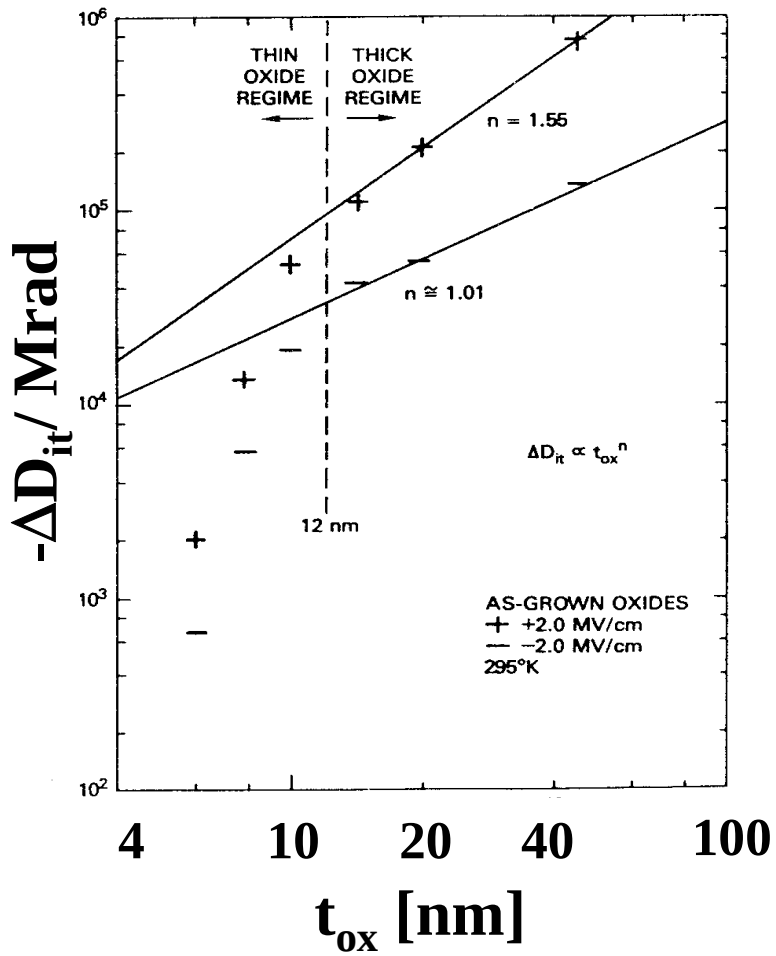
Total Dose damage and scaling





N. S. Saks et al., *IEEE TNS*, vol. 31, no. 6, Dec. 1984, and vol. 33, no. 6, Dec. 1986.

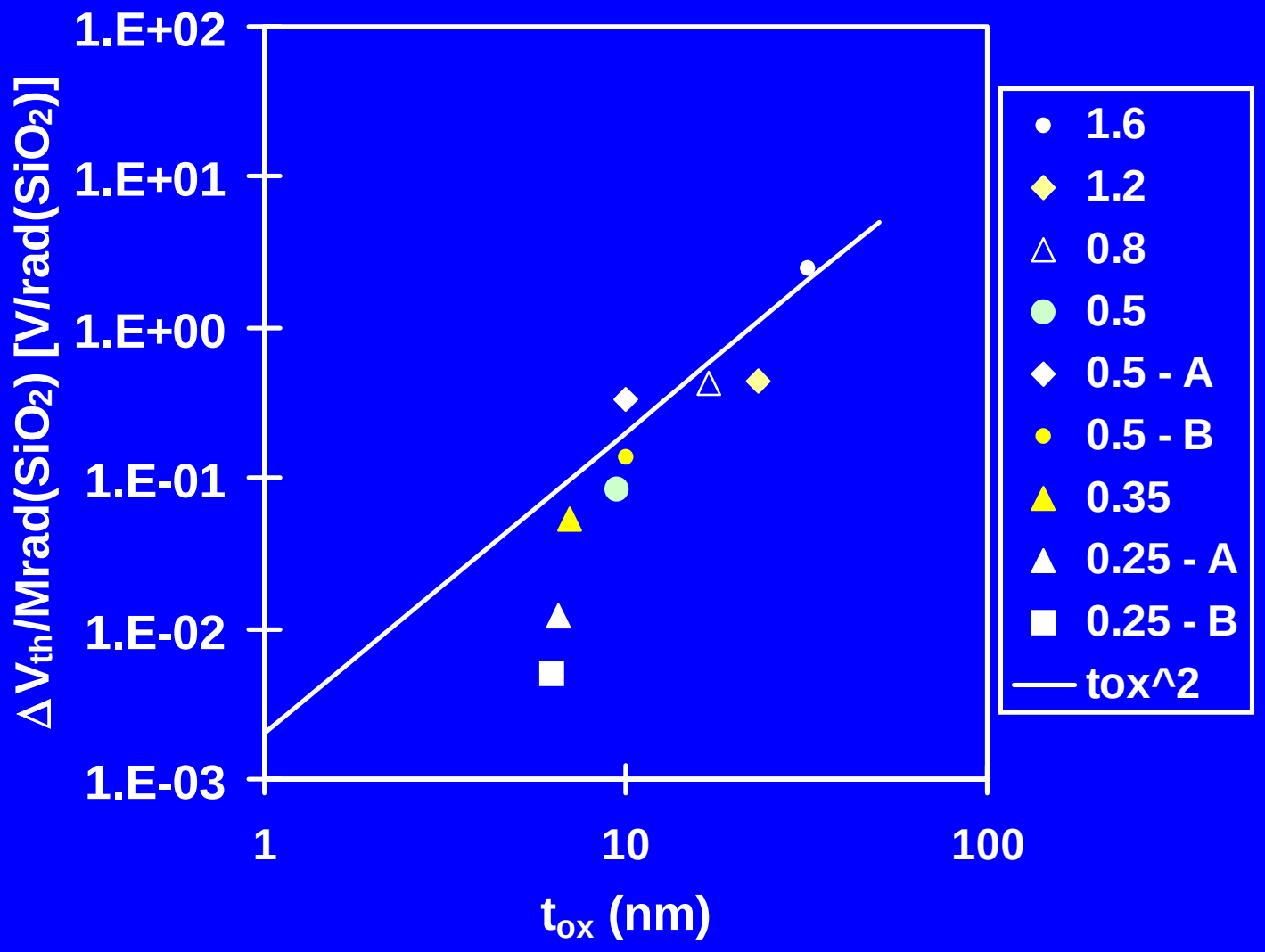
Total Dose damage and scaling

Decreasing t_{ox} we decrease the degradation of:

- ΔV_T, $\frac{\Delta V_T}{V_T}$, $\frac{\Delta V_T}{V_{DD}}$
- $\mu = \frac{\mu_0}{1+\alpha\cdot\left(\Delta N_{it}\right)}$
- **Transconductance**
- **Subthreshold slope**
- **Noise**

And the threshold voltage shift for n-channel transistors might not be negative anymore...

ΔV_T and t_{ox} scaling



SEL and scaling

Modern CMOS technologies have:

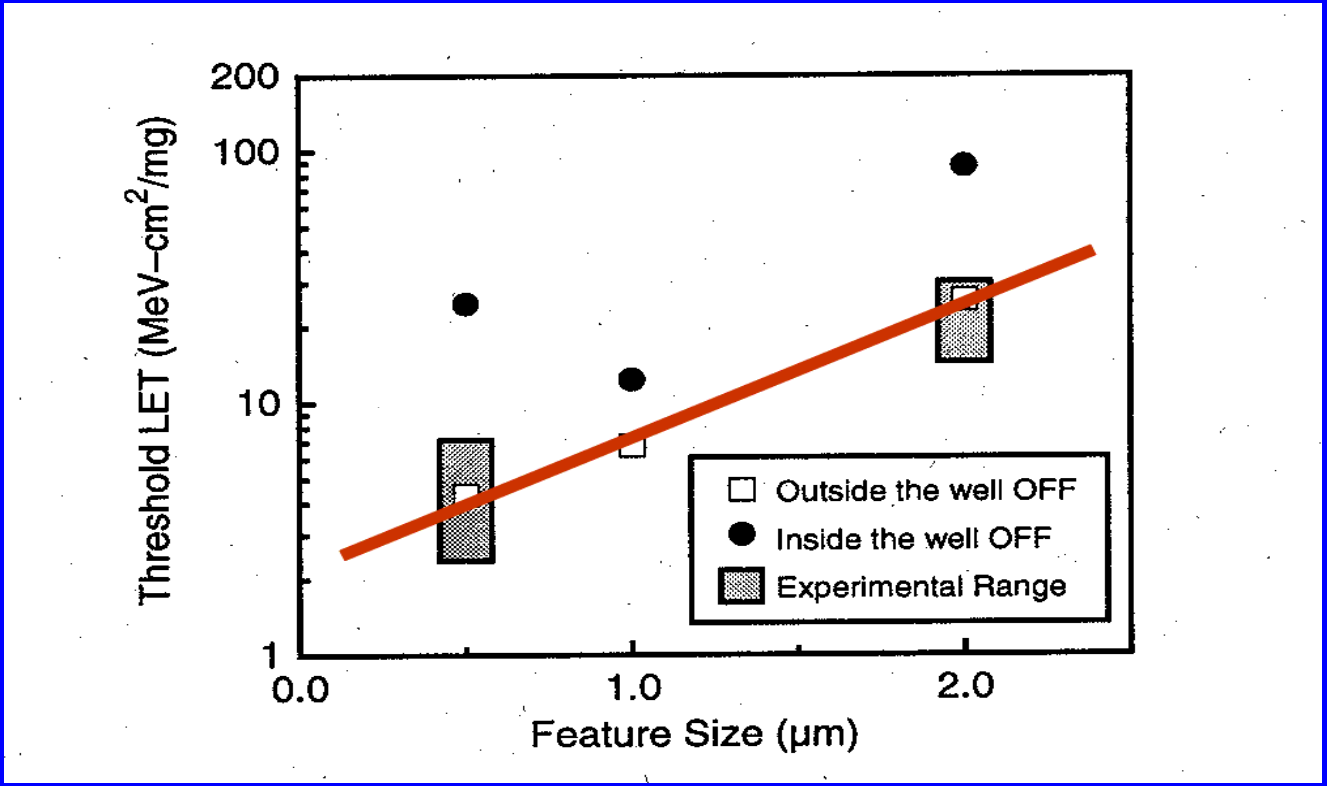
- **Retrograde wells**
- **Thinner epitaxial layers**
- **Trench isolation**
- **V_{DD} reduced**

All these issues help in preventing SEL, but they might not be always effective

A. H. Johnston, "The Influence of VLSI Technology Evolution on Radiation-Induced Latchup in Space Systems", *IEEE Transactions on Nuclear Science*, vol. 43, no. 2, Apr. 1996, pp. 505-521.

SEU and scaling

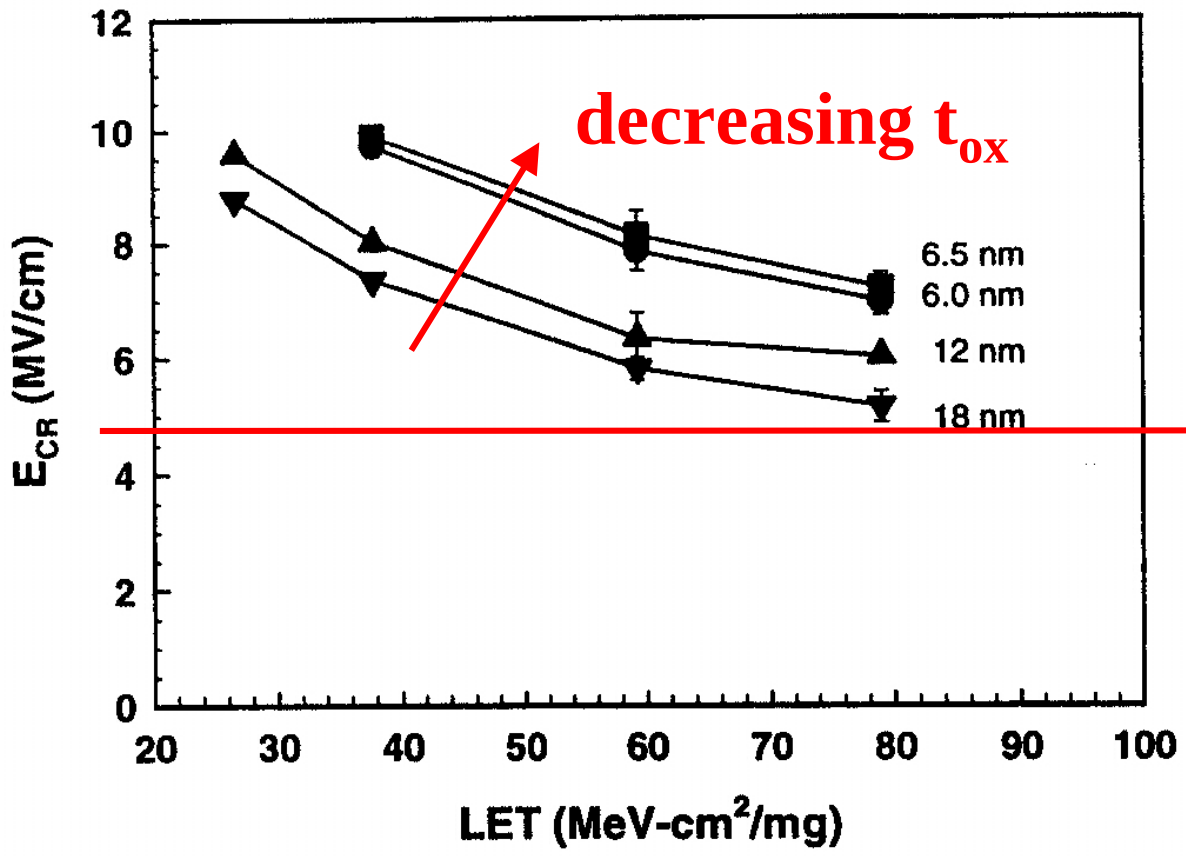
- V_{DD} reduced
- Node C reduced



P.E. Dodd et al., "Impact of technology trends on SEU in CMOS SRAMs", *IEEE Transactions on Nuclear Science*, vol. 43, no. 6, Dec. 1996, pp. 2797-2804.

The SEU problem worsen with scaling!

SEGR and scaling



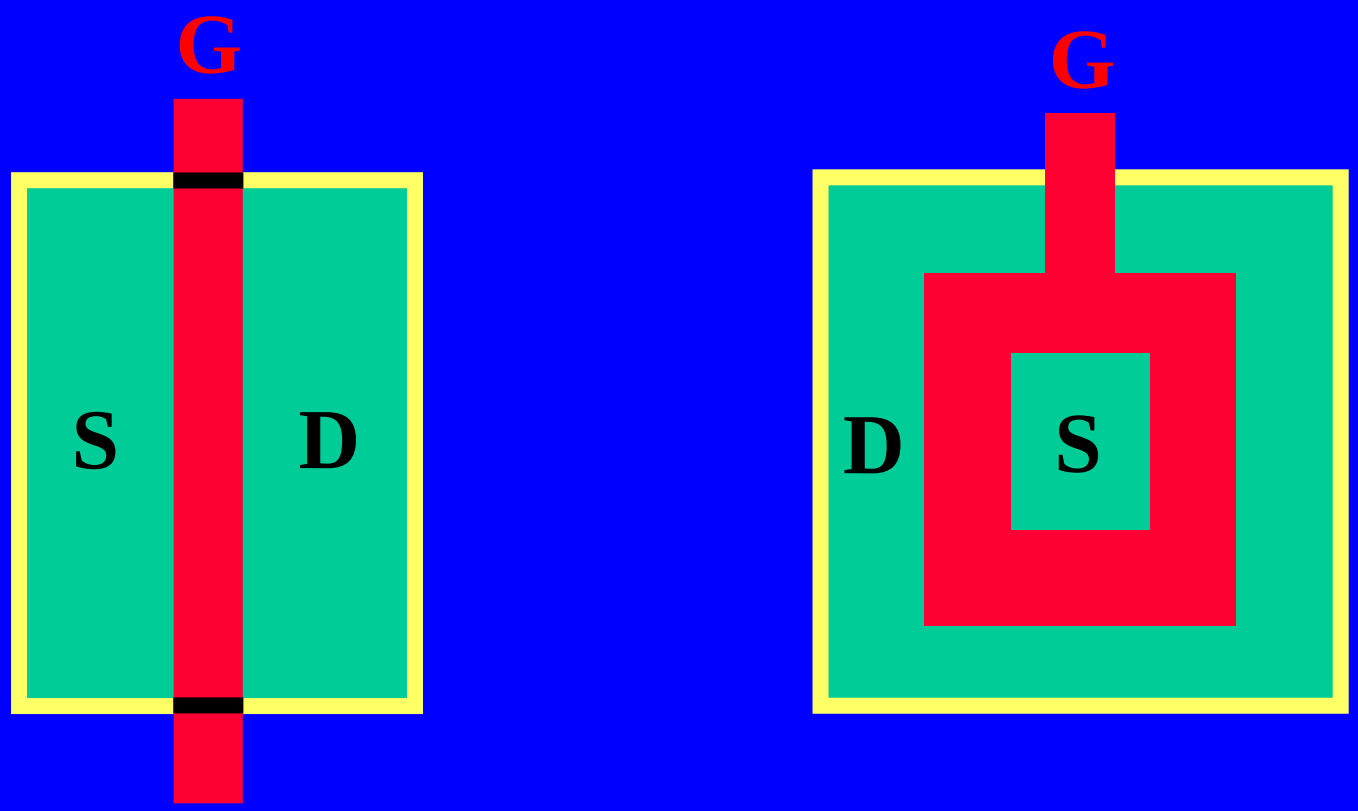
Maximum electric field for a quarter micron technology

F.W. Sexton, D.M. Fleetwood et al., "Single Event Gate Rupture in Thin Gate Oxides", *IEEE Transactions on Nuclear Science*, vol. 44, no. 6, December 1997, pp. 2345-2352.

Outline

- CMOS technologies
- The concept of scaling
- Scaling impact on device and circuit performance
- Ionizing radiation effects on CMOS ICs
- Scaling impact on radiation tolerance
- Radiation tolerant design
  - The Enclosed Layout Transistor (ELT)
  - The use of guard rings
  - SEE tests
- Circuit examples
- Conclusions

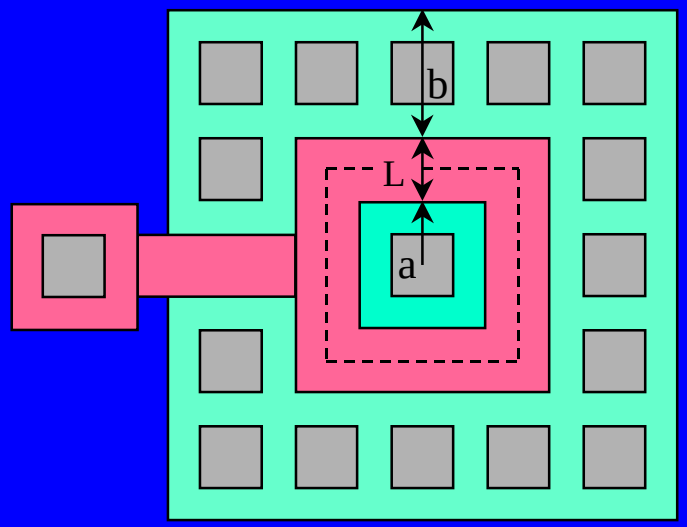
Enclosed Layout Transistor (ELT)



ELTs solve the leakage problem in the NMOS transistors

At the circuit level, guard rings are necessary

Drawbacks of ELTs



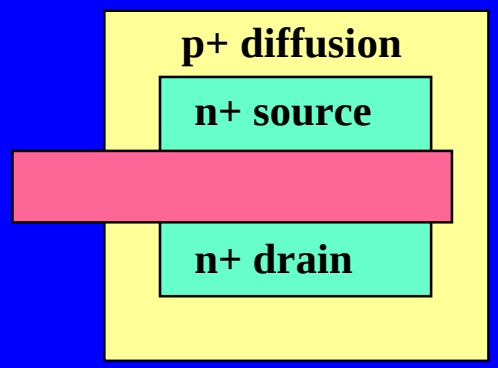
- Waste of area
- Increase in the parasitic gate and source/drain capacitance
- Modeling problems
- Lack of symmetry
- Balancing of n- and p-channel

$W = 8a + 4L$

$W/L = 8a/L + 4$

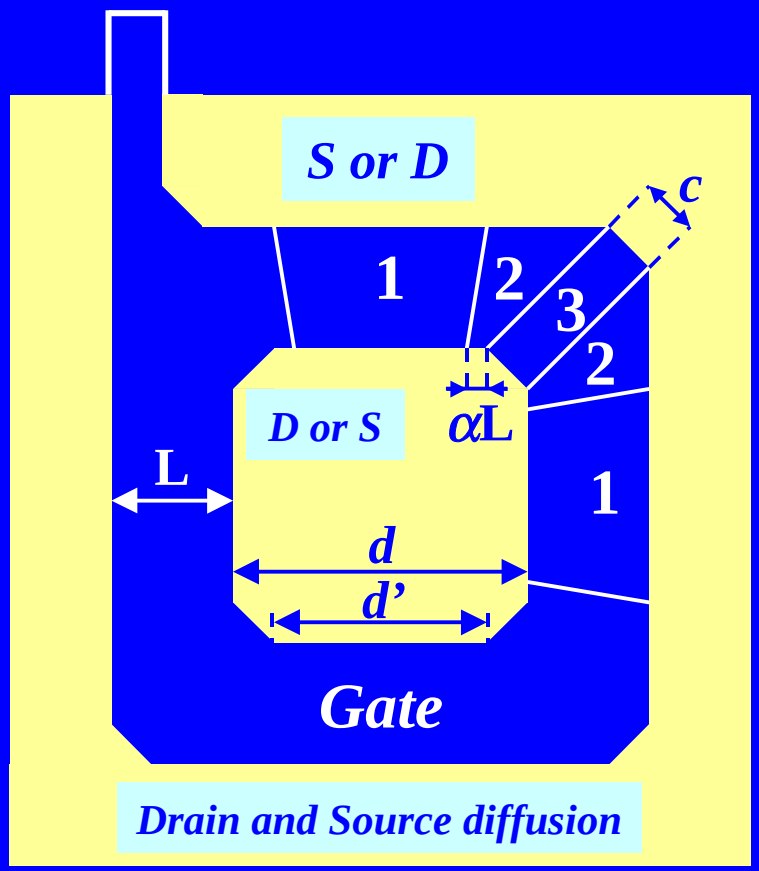
$\text{Area} = 4(a+b+L)^2$

Another possible solution?



Aspect ratio modeling

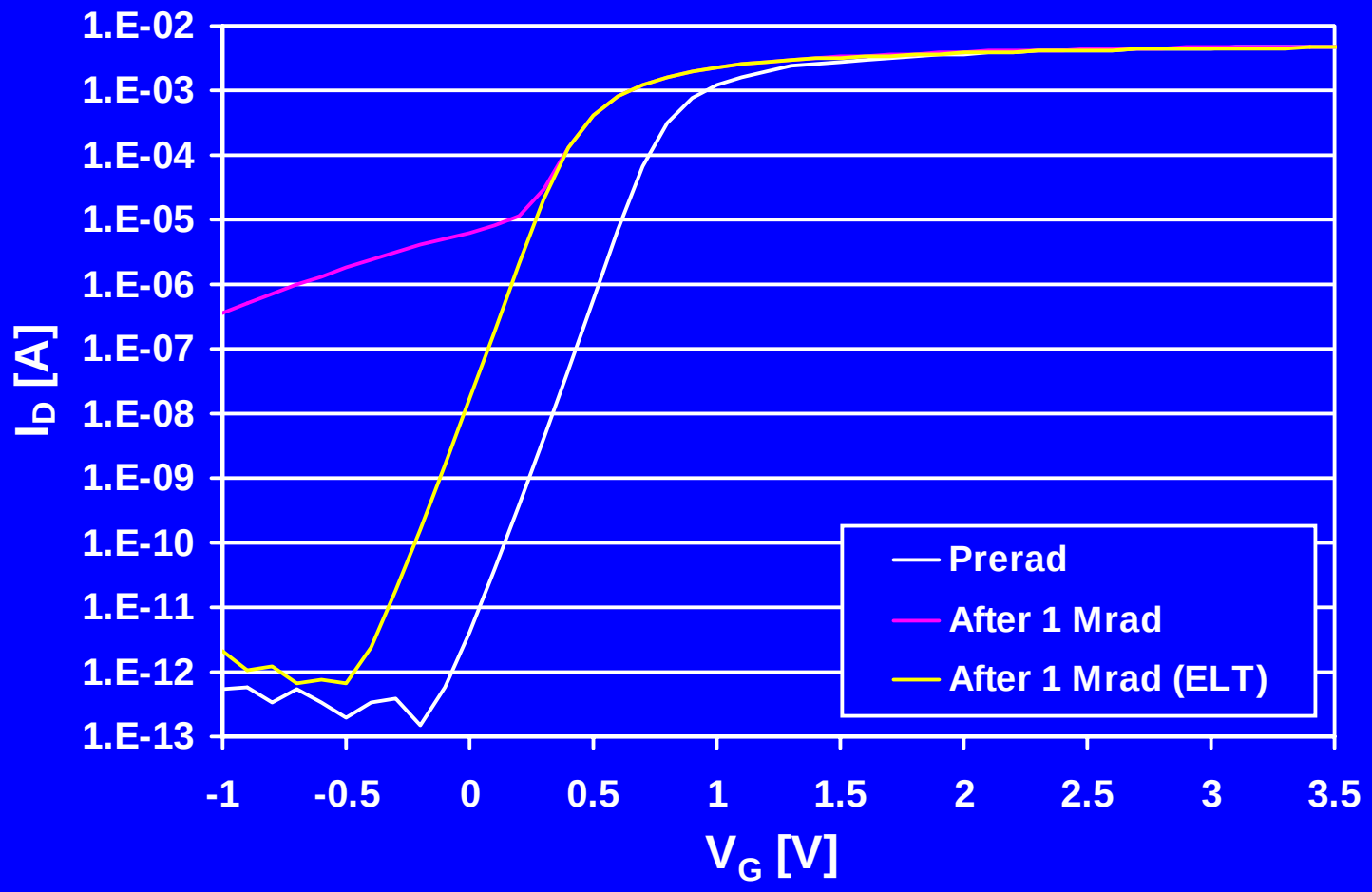
$$\frac{W}{L} = \underbrace{4\,\frac{2\alpha}{\ln\frac{d'}{d'-2\alpha L}}}_{1} + \underbrace{2K\,\frac{1-\alpha}{\frac{1}{2}\sqrt{\alpha^2+2\alpha+5}\cdot\ln\frac{1}{\alpha}}}_{2} + \underbrace{3\,\frac{\frac{d-d'}{2}}{L}}_{3}$$



L (μm)	Calc. W/L	Extr. W/L
0.28	14.8	15
0.36	11.3	11.2
0.5	8.3	8.3
1	5.1	5.2
3	3	3.2
5	2.6	2.6

A. Giraldo et al., "Aspect ratio calculation in n-channel MOSFETs with a gate-enclosed layout", *Solid-State Electronics*, vol. 44, June 2000, pp. 981-989.

Effectiveness of ELTs



0.7 μm technology - t_{ox} = 17 nm

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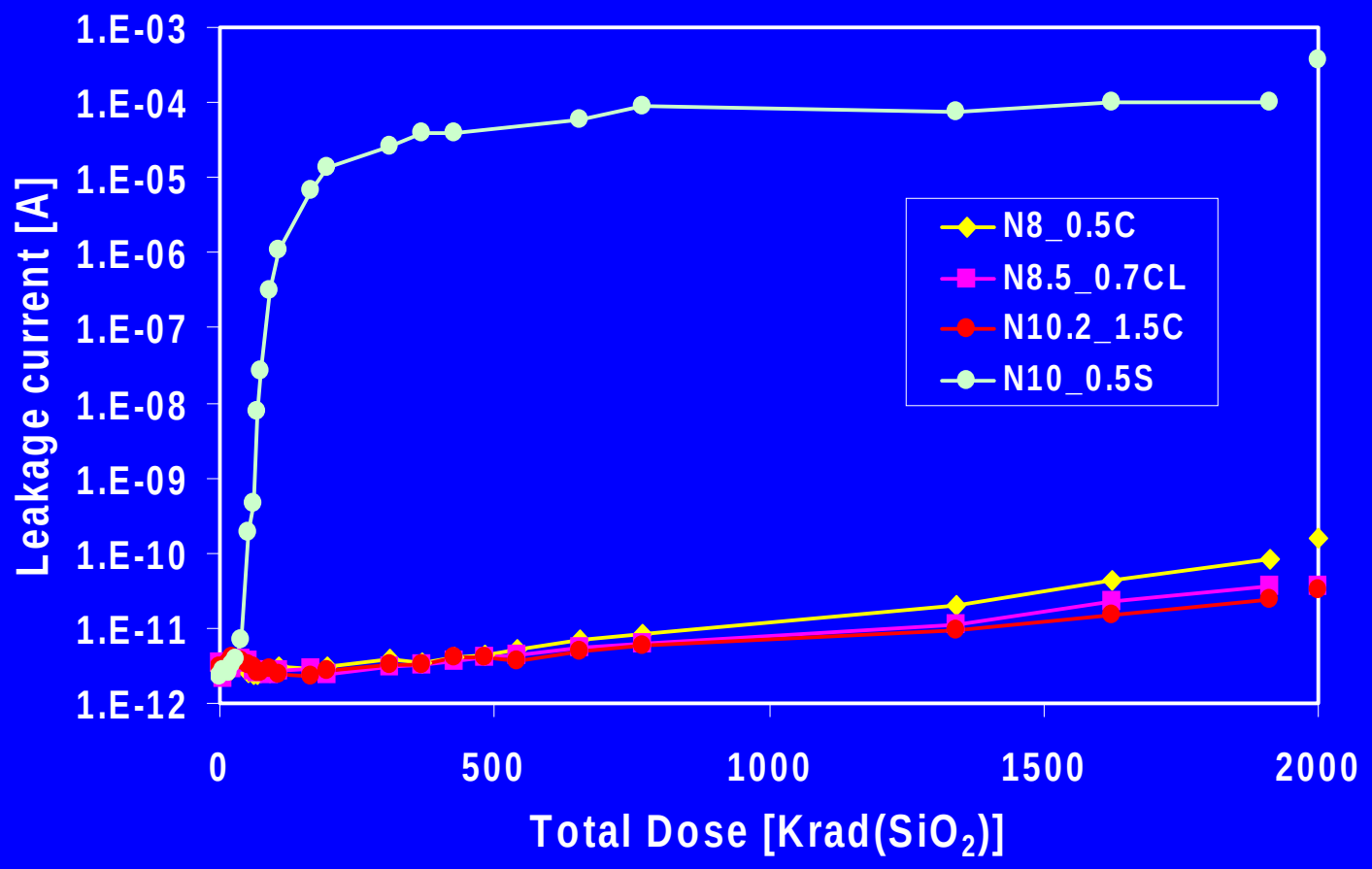
Effectiveness of ELTs



0.5 μm technology - t_{ox} = 10 nm

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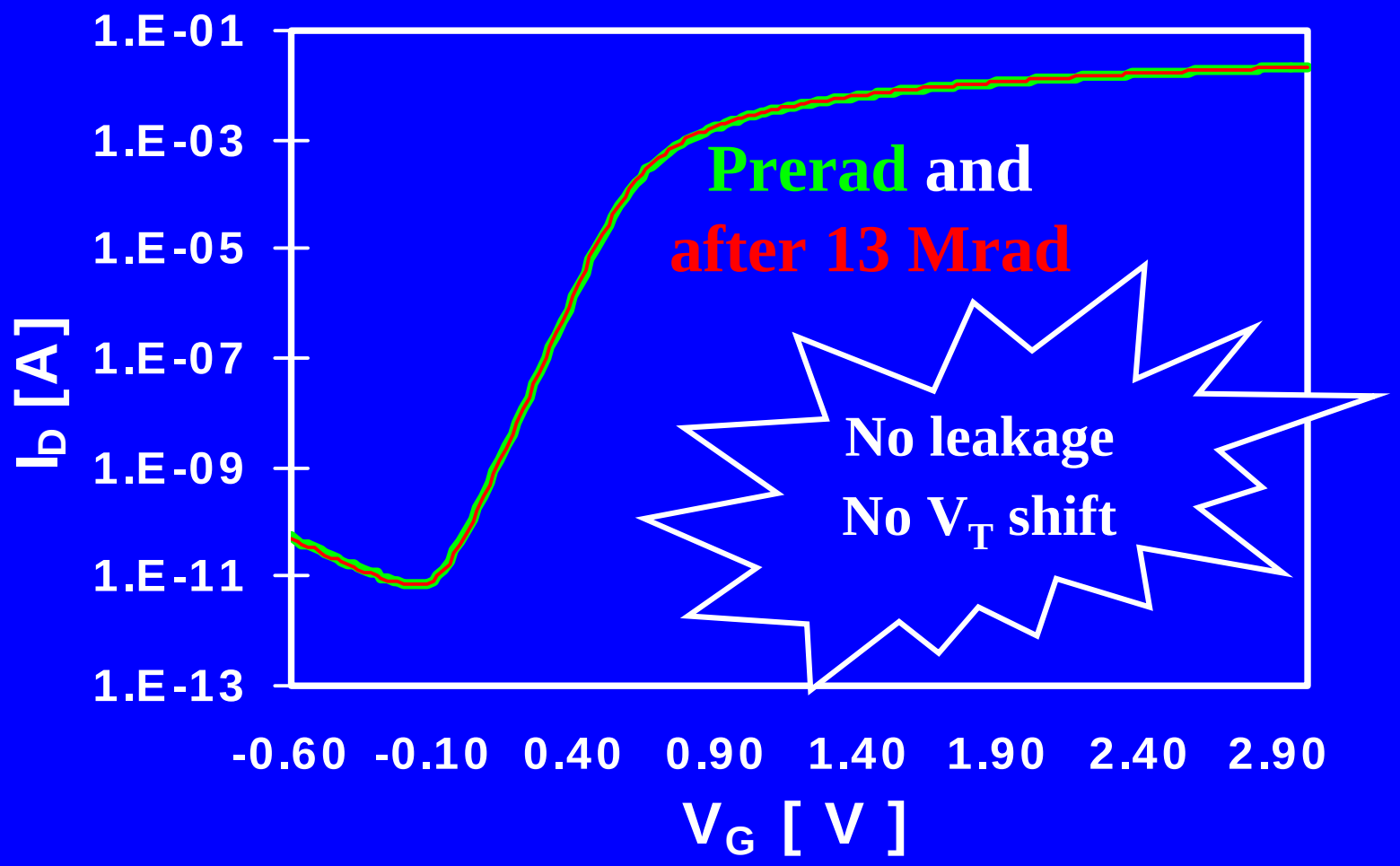
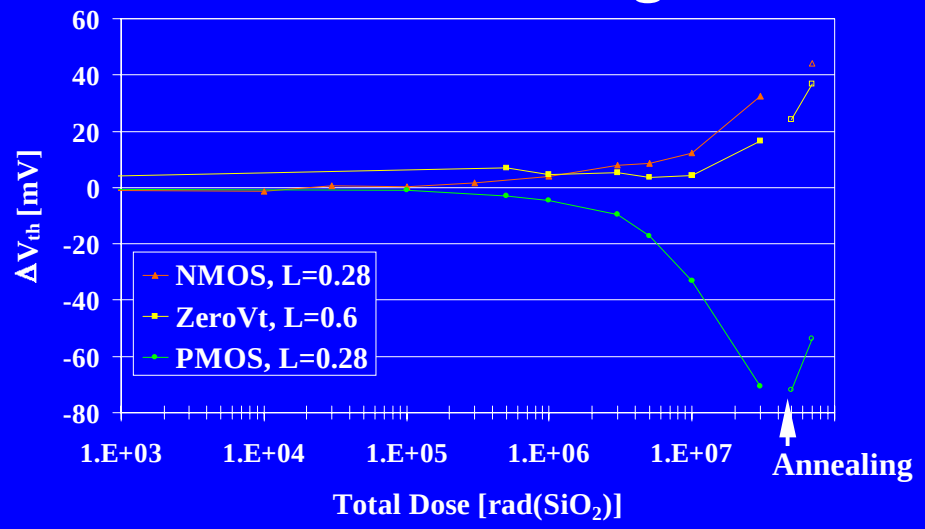
ELT & deep submicron



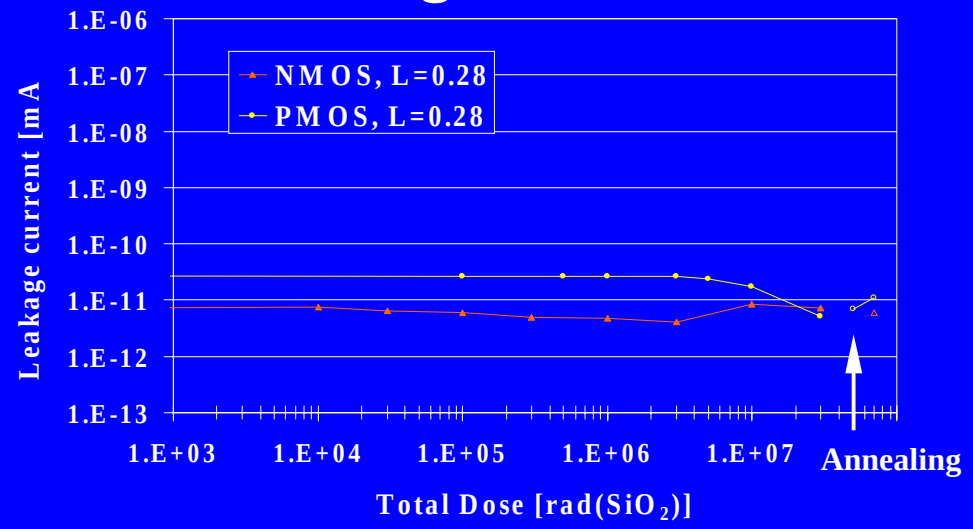
0.25 μm technology - t_{ox} = 5 nm

Total dose results up to 30 Mrad

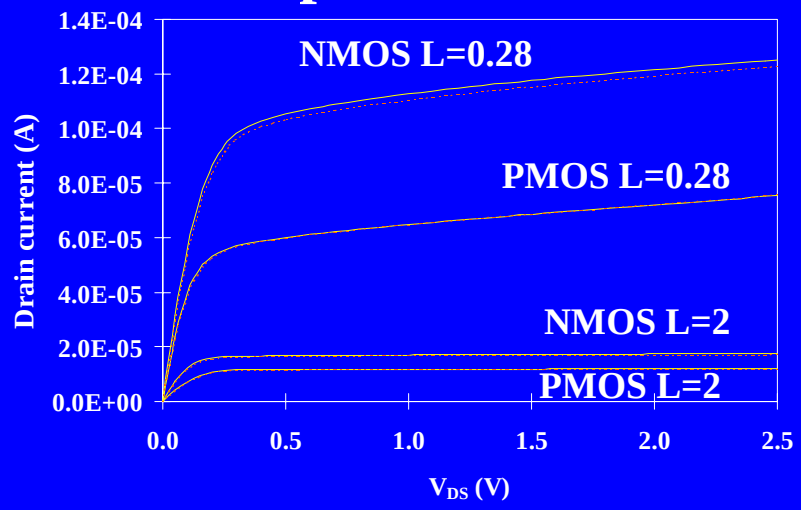
Threshold voltage



Leakage current



Output conductance



Mobility degradation:

< 6% NMOS

< 2% PMOS

0.25 µm technology

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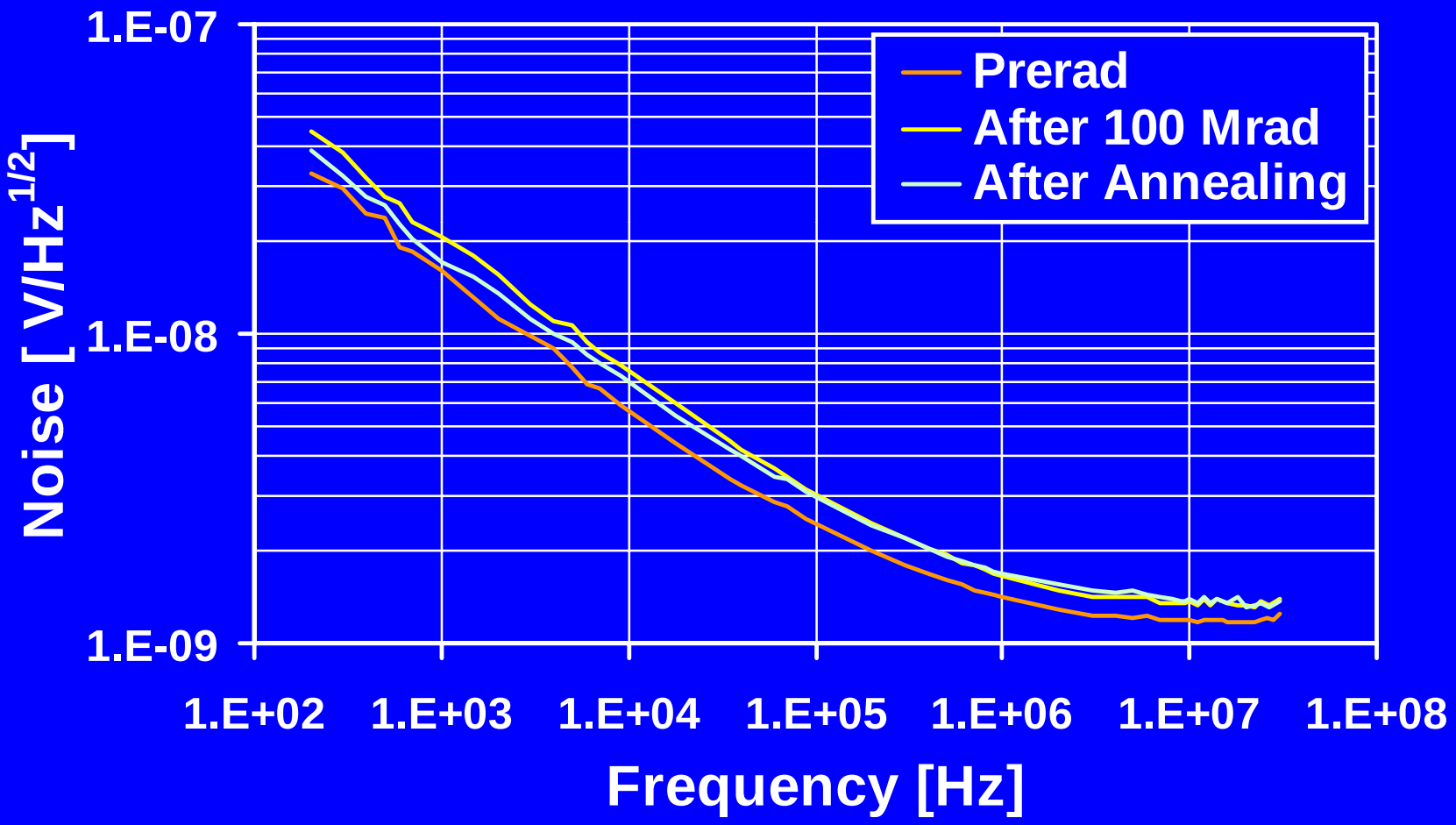
N-channel noise spectrum



0.25 μm technology - t_{ox} = 5 nm

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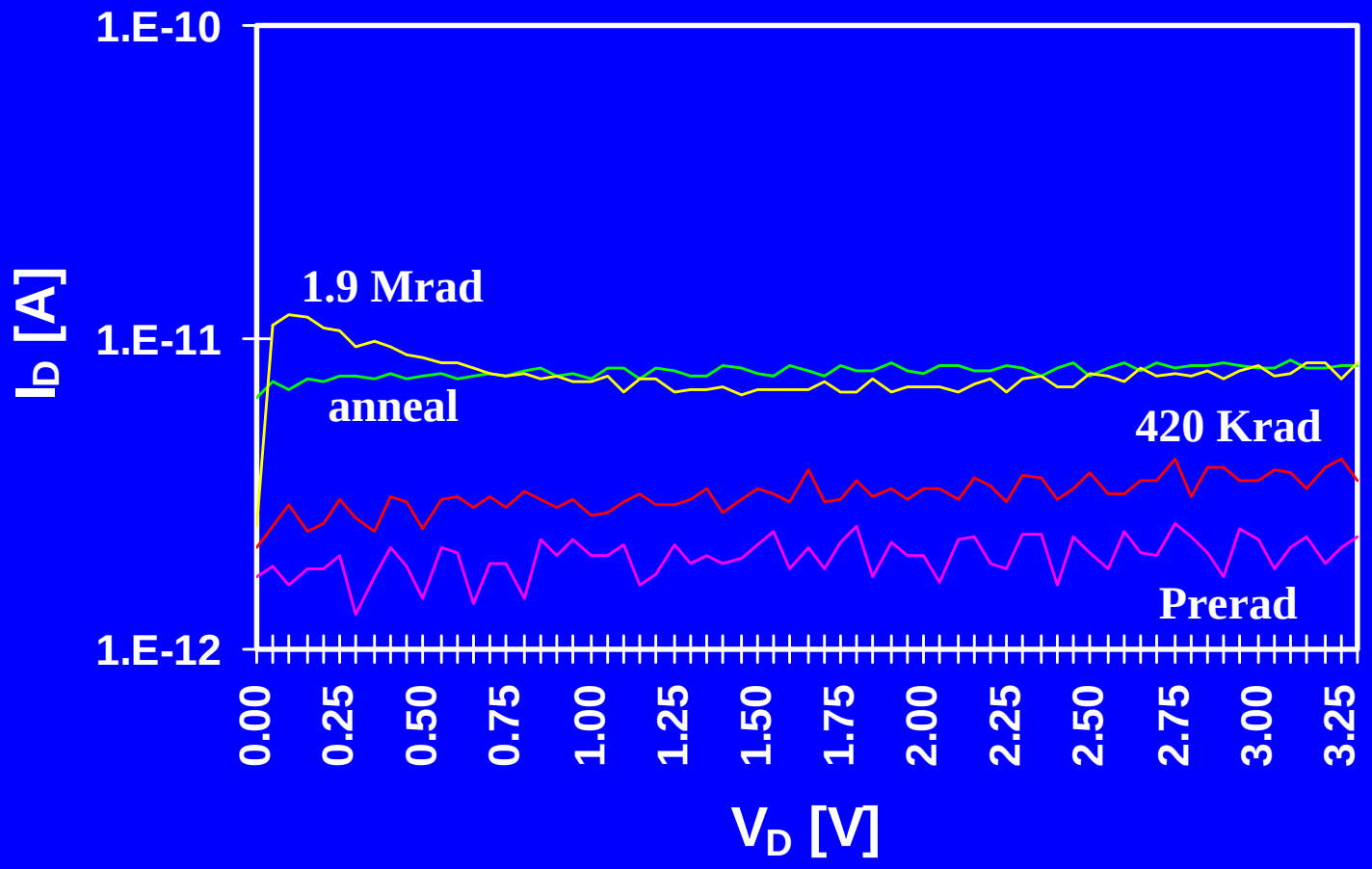
Field oxide leakage



FOXFET 14.4/2.6 without gate, with guardring
0.5 μm technology

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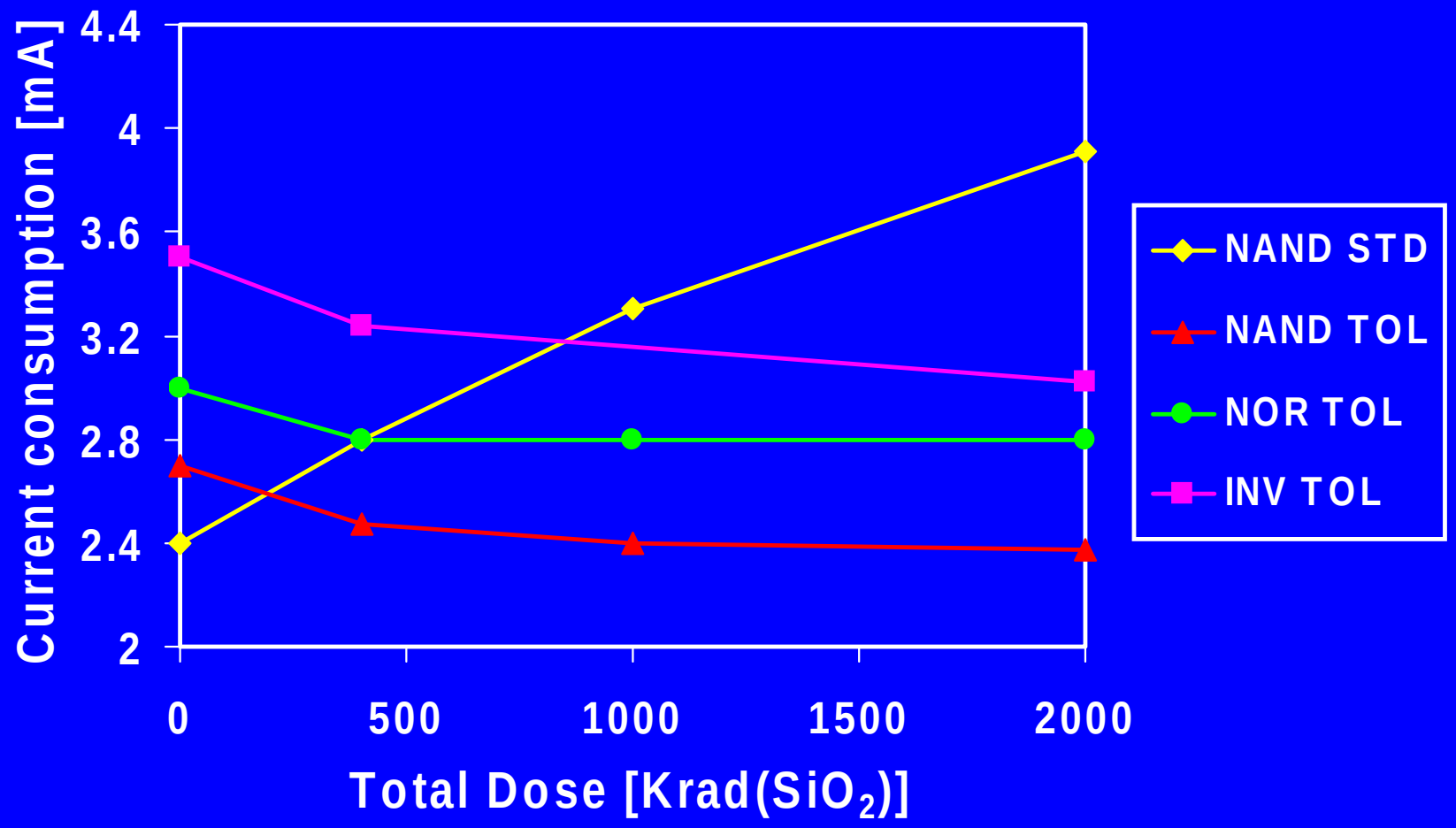
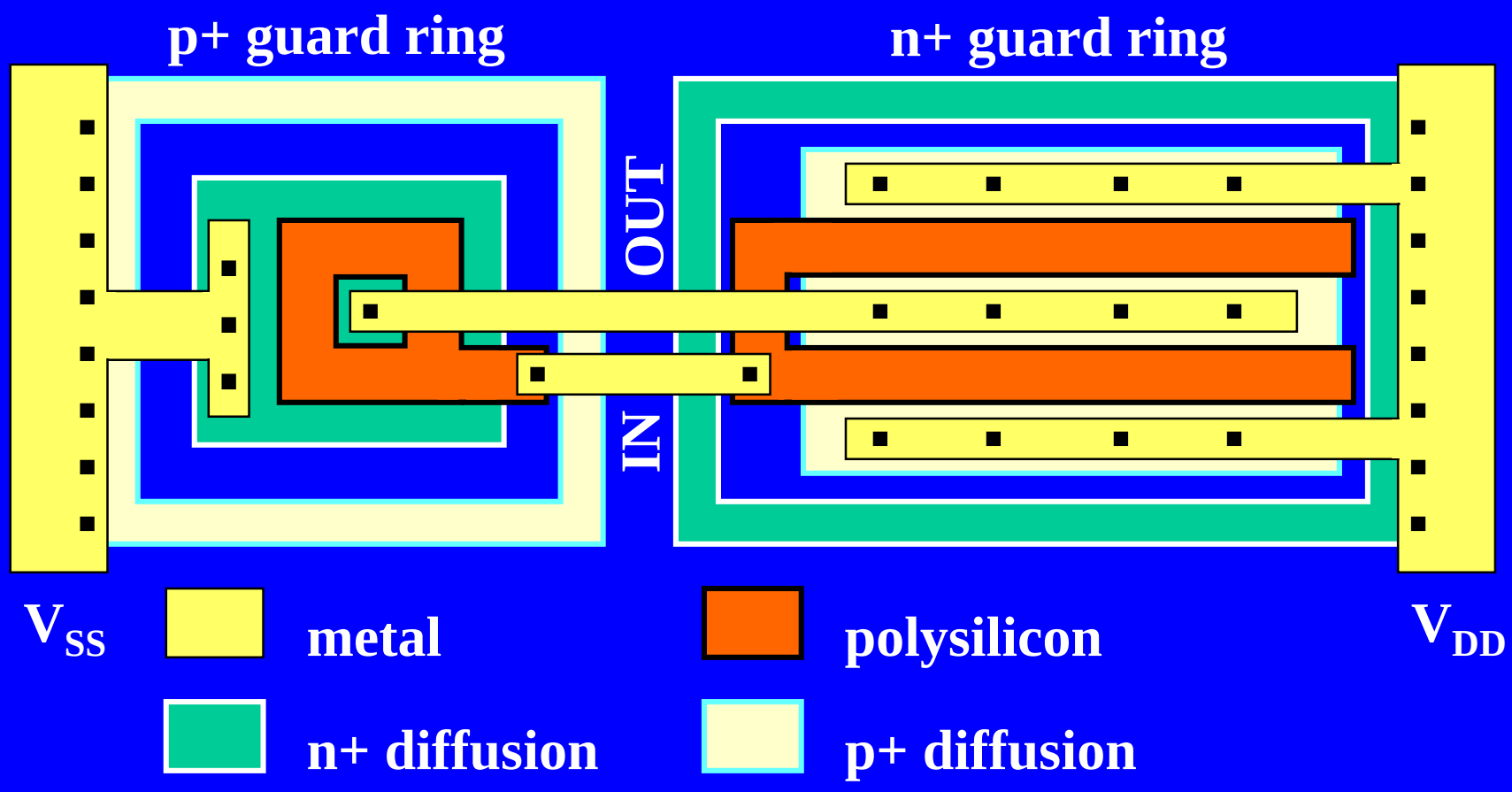
Ring oscillators (49 inverters)



0.5 μm technology

Radiation tolerant layout approach



SEL and SEGR tests

SEL

The systematic use of guard rings is an effective tool against SEL

NO latch-up observed up to 89 MeVcm^{2}mg^{-1}

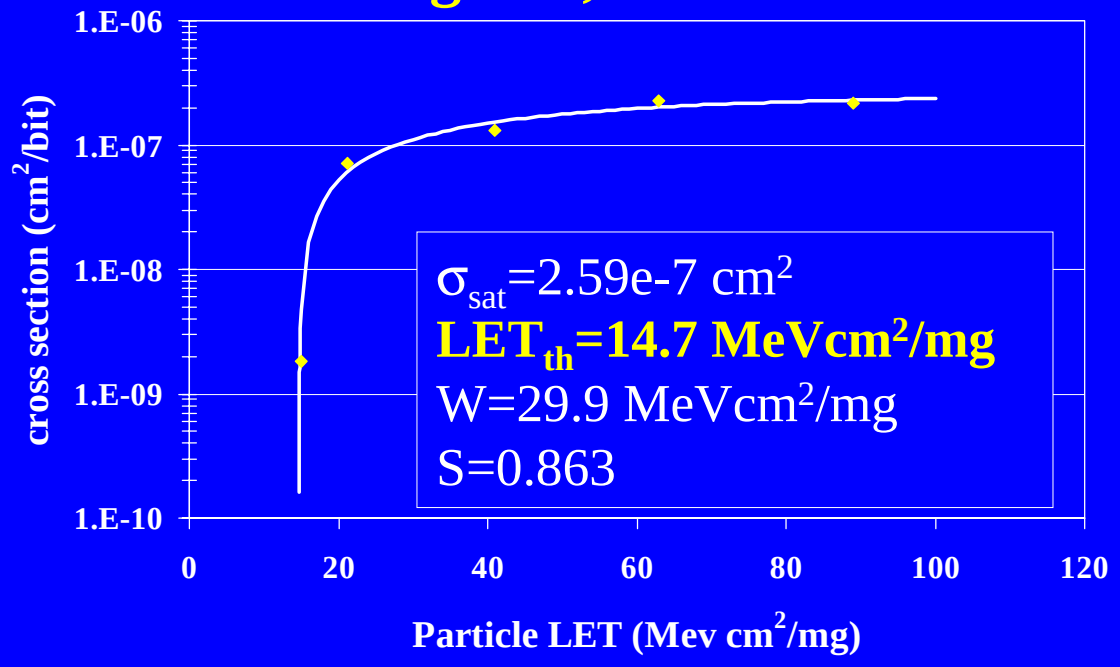
F. Faccio et al., "Single Event Effects in Static and Dynamic Registers in a 0.25 µm CMOS Technology", *IEEE Transactions on Nuclear Science*, vol. 46, no. 6, Dec. 1999 , pp. 1434-1439.

SEGR

NEVER observed in our circuits

Single Event Upset tests

Static register, un-clocked mode



$$\sigma = \frac{N_{events}}{\Phi \cdot N_{bits}} \ (cm^2/bit)$$

Design hardened register: LET_{th} between 63 and 89 $MeVcm^2mg^{-1}$

at 89 $MeVcm^2mg^{-1}$, $\sigma < 10^{-8}$ cm^2/bit

F. Faccio et al., "Single Event Effects in Static and Dynamic Registers in a 0.25 µm CMOS Technology", *IEEE Transactions on Nuclear Science*, vol. 46, no. 6, Dec. 1999 , pp. 1434-1439.

Comparison with the general trend

This static cell

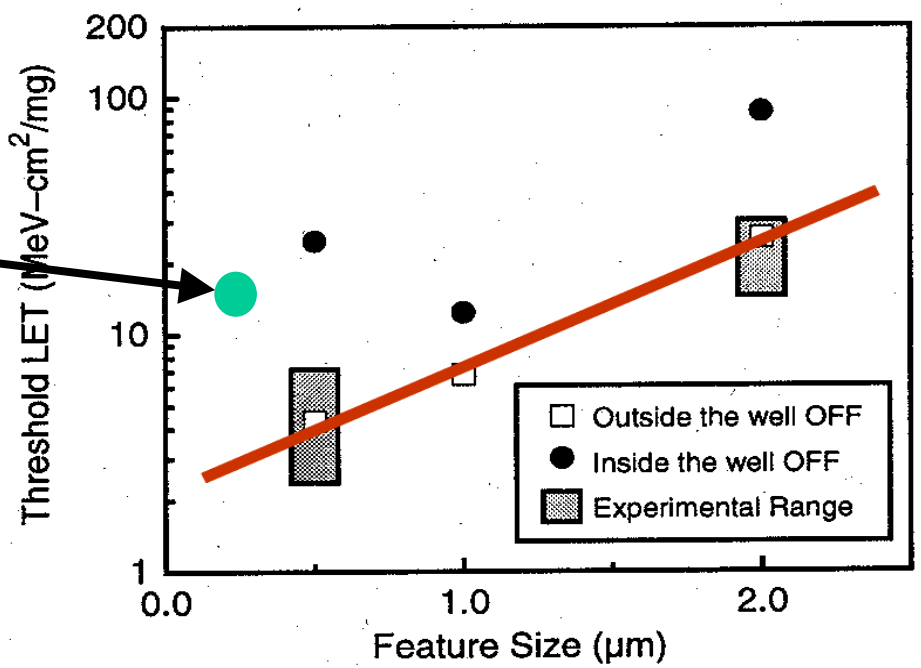
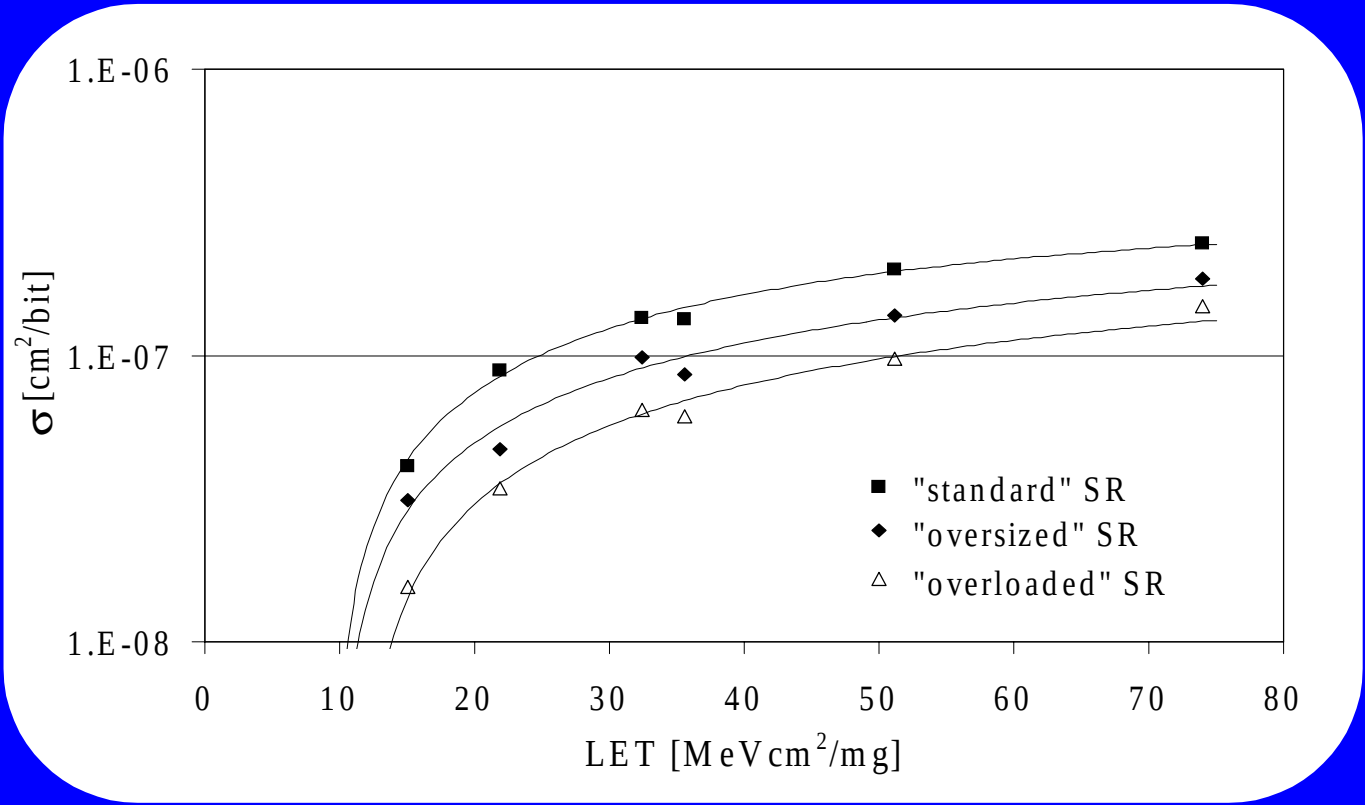


Figure 5. Experimentally–measured and simulated upset thresholds in three Sandia SRAM technology generations (no feedback resistors). The 1– and 2–µm technologies are n–substrate, 5 V; the 0.5–µm technology is p–substrate, 3.3 V.

P.E. Dodd et al., "Impact of technology trends on SEU in CMOS SRAMs", *IEEE Transactions on Nuclear Science*, vol. 43, no. 6, Dec. 1996, pp. 2797-2804.

SEU in 3 static shift registers



Upset rates:

twofold decrease for the “oversized”
tenfold decrease for the “overloaded”

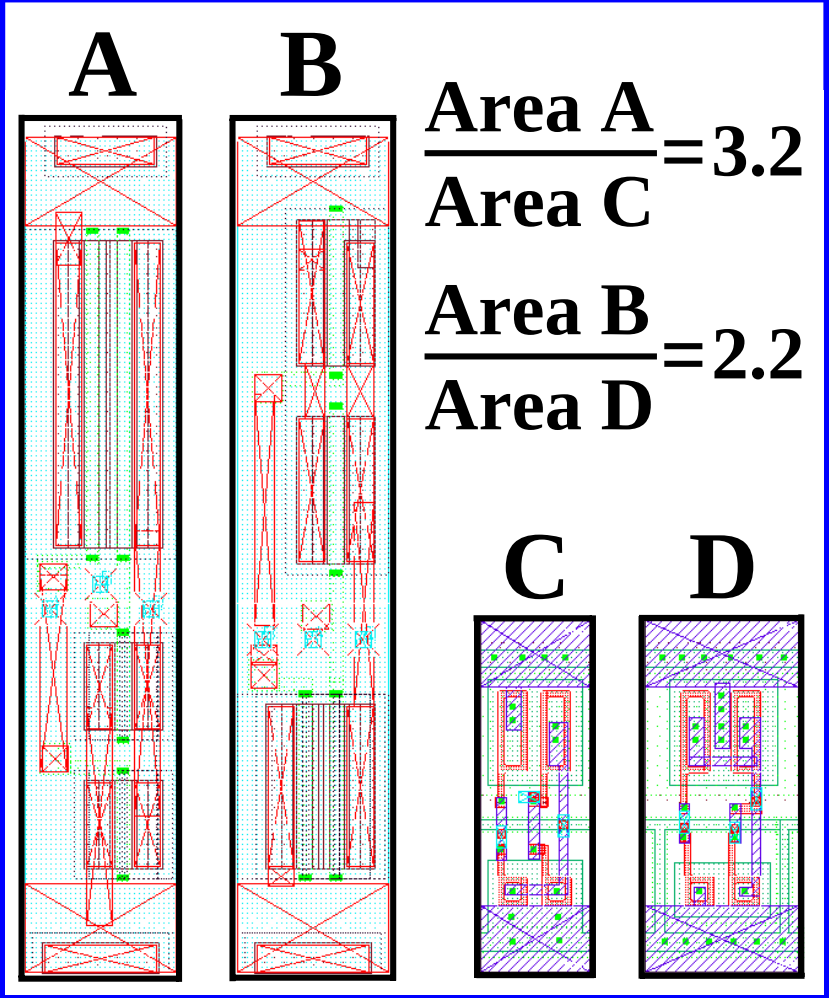
Radiation tolerant layout approach

$\Delta V_{th} \propto t_{ox}^{n}$ + ELT's and guard rings = TID Radiation Tolerance

Deep sub-µm means also:

- speed
- low power
- VLSI
- low cost
- high yield

Density and speed



$$\frac{\text{Area A}}{\text{Area C}} = 3.2$$

$$\frac{\text{Area B}}{\text{Area D}} = 2.2$$

A & B : 0.6 μm standard

C & D : 0.25 μm rad-tol

Inverter with F.O. = 1

	0.6 μm	0.25 μm
V_{DD} [V]	3.3	2
Delay [ps]	114	48
Pwr [μW/MHz]	1.34	0.14
Area [μm^2]	162	50

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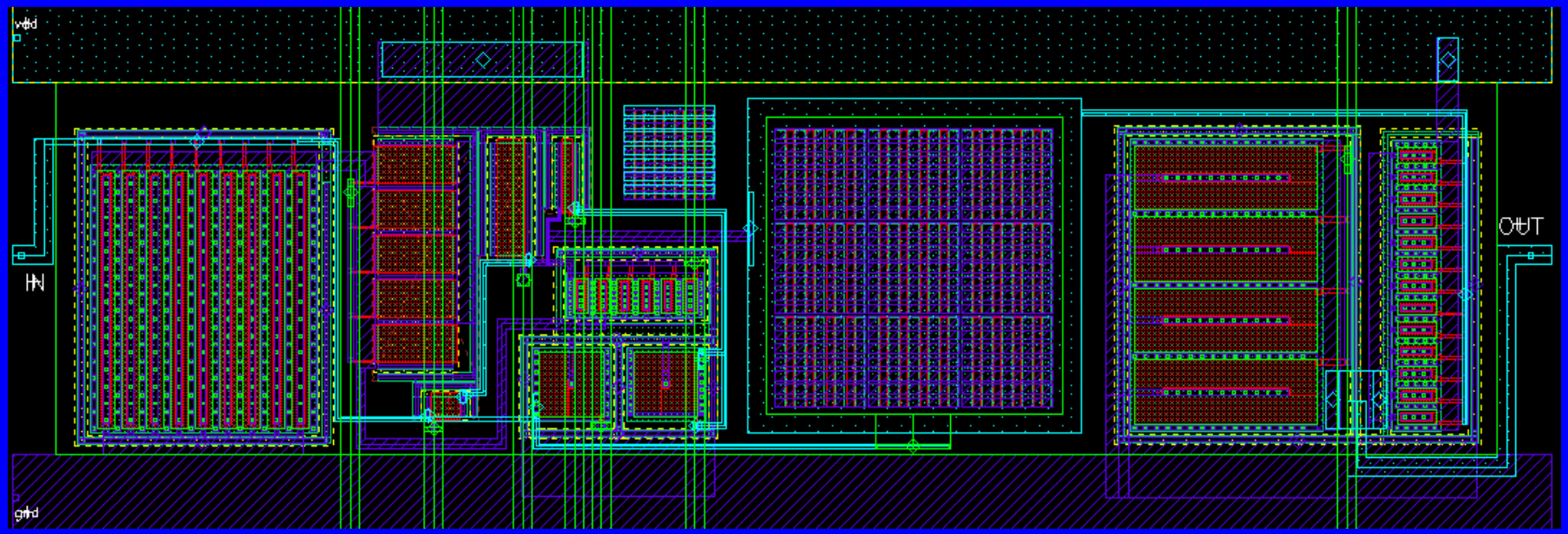
NA60 proton beamscope chip

Layout of a fast charge amplifier used to read the signals coming from a microstrip detector

50 μm * 150 μm



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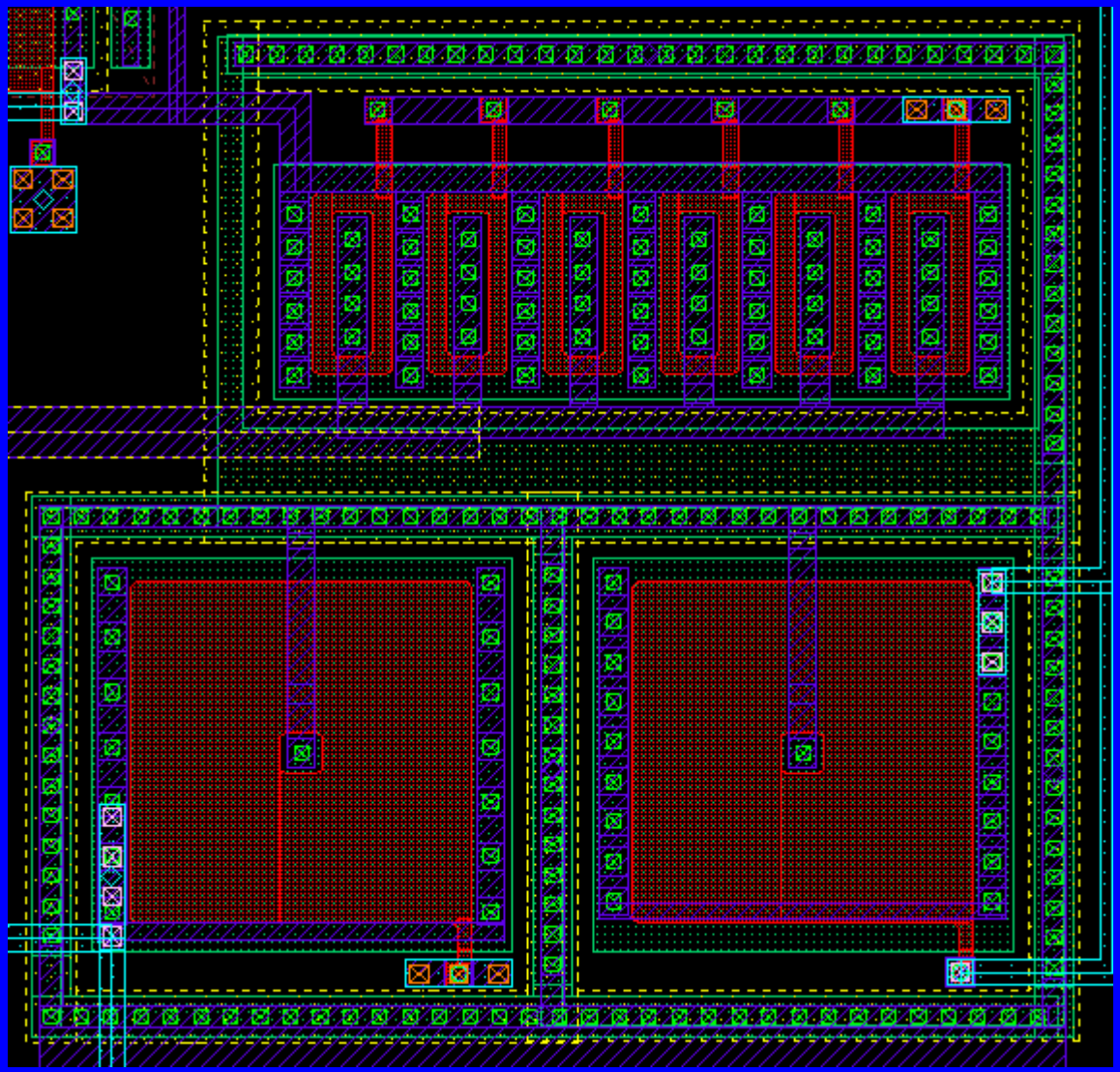
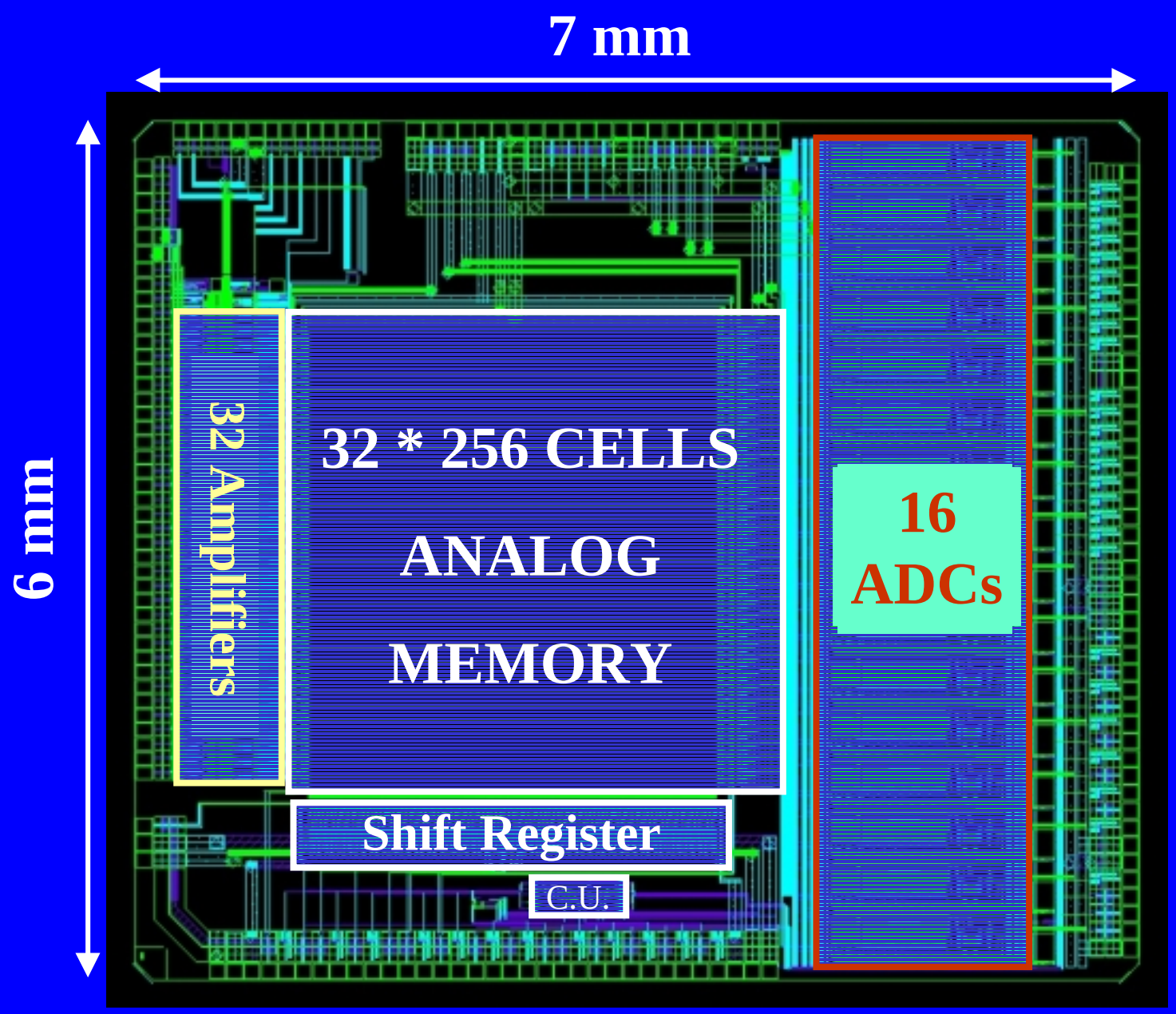
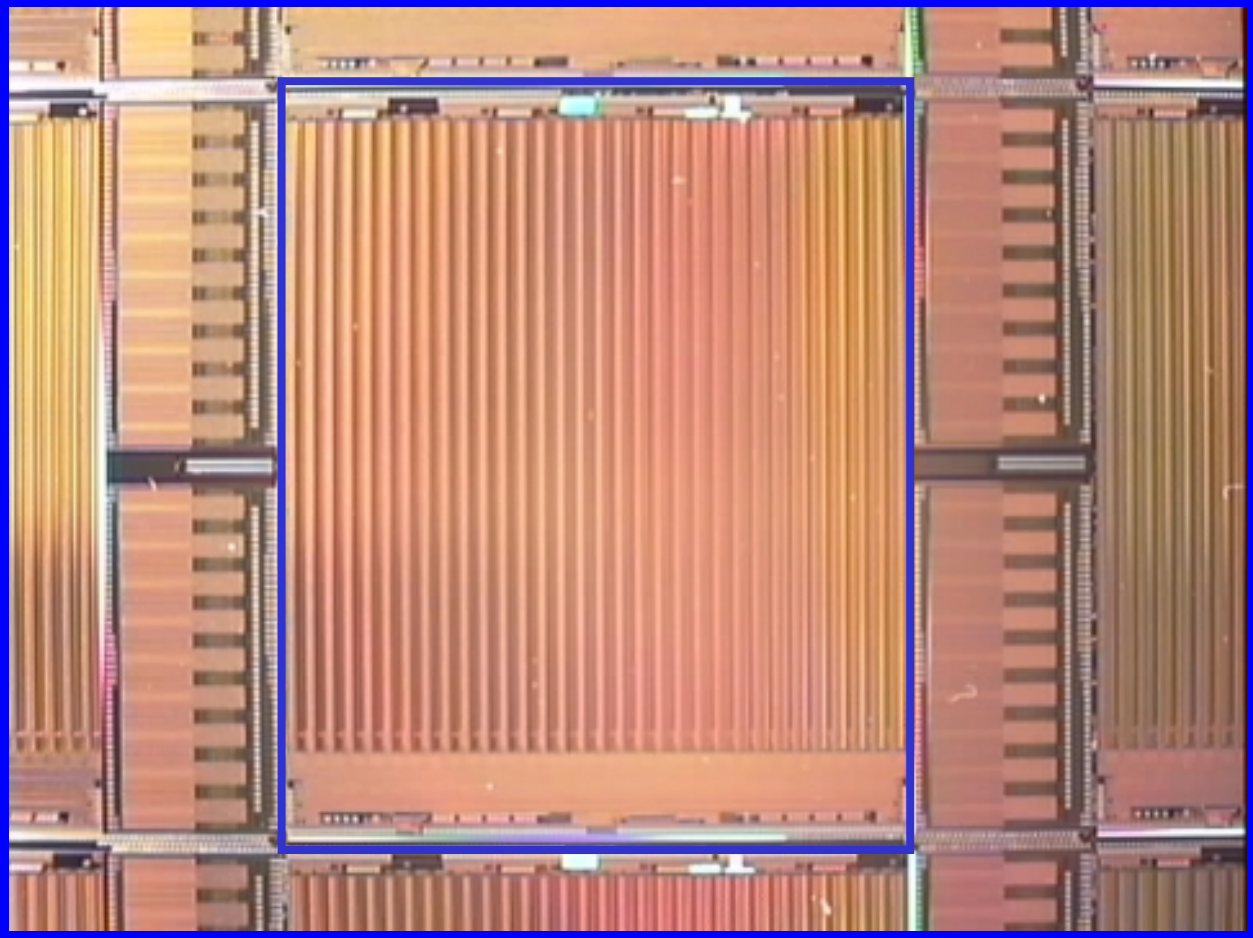
Layout detail





ALICE SDDs readout chip

The ALICE1LHCb pixel chip



Full chip 8192 readout channels

13 M transistors in 14 by 16 mm^2

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Conclusions

- CMOS technologies are (and will be) the most widespread in the IC world: it is therefore convenient for us to use them
- They can be used to make radiation tolerant circuits (with some special tricks...)
- To continue to use them in the future for HEP experiments several new problems will have to be addressed, such as how to make analog circuits with ULSI CMOS technologies

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Last but not least, have a look at: http://www.cern.ch/RD49

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